MB86R01

DATA SHEET

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FUJITSU

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Revision History

Date	Ver.	Contents
2007/07/12	1.0	Newly issued
2007/08/20	1.1	8.3.1. Recommended Power On/Off Sequence • Revised the last line of description (PLL reference clock part) 8.4.3. ADC • Revised value of table 8-16 • Revised and deleted descriptive content of note • Revised footnote (*2) of table 8-17 8.4.4. I^2C Bus Fast Mode I/O • Revised table 8-18 and footnote • Deleted footnote (*3) 8.5.9. I^2C Bus Timing • Revised footnote (*2) of table 8-37 8.5.12. MLB Signal Timing • Revised MLB to MediaLB • Revised footnote of table 8-42, 8-45
2007/11/09	1.2	4. Function list • Revised contents of the list 6. Pin assignment • Revised figures in 1-8/1-9 pages • Added "top view" statement 7.1. Pin Multiplex • Revised description of note • Added mode setting description to pin multiplex group #1 ~ #5 • Revised table of pin multiplex group #2 and #4 7.2.4. USB 2.0 Host/Function related pin • Revised description of USB_EXT12K pin 7.2.5. External interrupt controller related pin • Revised title 7.2.12. A/D converter related pin • Revised pin name: AD_AVD0 → AD_AVD, AD_AVS1 → AD_AVS 7.2.24. Unused pin • Added this section 7.2.25. Unused pin with pin multiplex function in the duplex case • Added this section 8.4.2. DDR2SDRAM IF I/O (SSTL_18) • Revised table 8-12 8.5.1. Memory Controller Signal Timing • Revised table 8-21 • Revised figure 8-8 and 8-9 • Added figure 8-10, 8-11, and 8-12 8.5.6.2. Input Signal • Revised figure 8-23
2008/02/07	1.3	6. Pin assignment • Revised figure and table 7.2.2. IDE66 related pin • Revised type • Revised status pin after reset 7.2.3. SD memory controller related pin • Unified SD_DAT[0] and SD_DAT[3:1] 7.2.7. CAN related pin • Revised type

Date	Ver.	Contents
2008/02/07	1.3	7.2.8. I2S related pin • Revised type • Revised status pin after reset 7.2.10. SPI related pin • Revised type 7.2.11. PWM related pin • Revised type • Added comment 7.2.13. DDR2 related pin • Revised resistance value of *2 7.2.15. Video captured related pin • Revised type • Added comment 7.2.18. ICE related pin • Revised status pin after reset of XSRST 7.2.20. ETM related pin • Revised pin name in description column of TRACECLK 7.2.22. MediaLB related pin • Revised pin name • Revised type 7.2.24. Unused pin • Revised process • Deleted BIGEND • Revised pin name of B17, B16, C17, C16, and D16 7.2.25. Unused pin with pin multiplex function in the duplex case • Revised process 8.1. Maximum Ratings • Revised table 8-1
2009/07/07	1.4	7.2.14. DISPLAY related pin • Added note 8.1. Maximum Ratings • Revised table 8-1 8.3.2. Power On Reset • Revised figure 8-3 • Revised description 8.5.5.1. Clock • Revised table 8-28 8.5.7. I2S Signal Timing • Revised table 8-34 and 8-35 8.5.10. SPI Signal Timing • Revised table 8-38

Contents

1. Outline

MB86R01 is LSI product for the graphics applications with ARM Limited's CPU ARM926EJ-S and Fujitsu's GDC MB86296 as its core. This product contains peripheral I/O resources, such as in-vehicle LAN, HDD, and USB; therefore only a single chip of MB86R01 controls main graphics application system which usually requires 2 chips (CPU and GDC.)

2. Feature

- CMOS 90nm technology
- Package: PBGA484
- Power-supply voltage: (IO: 3.3 ± 0.3V, core: 1.2 ± 0.1V, DDR2: 1.8 ± 0.1V)
- Operation frequency: 333MHz (CPU), 83MHz (AHB), 41.5MHz (APB)
- CPU core
  - ARM926EJ-S
  - 16KB instruction cache/16KB data cache
  - 16KB ITCM/16KB DTCM
  - ETM9CS Single and JTAG ICE interface
  - Java acceleration (Jazelle technology)
- Bus architecture
  - Multi-layer AHB bus architecture
- Interrupt
- Built-in SRAM
- Clock/Reset control function
- Remap/Boot control function
- 16 bit external bus interface with decoding engine
- 32 bit DDR2 memory interface (target: 166MHz: 333Mbps)
- Graphics display controller
  - 2D/3D rendering engine of Fujitsu MB86296
  - RGB66 video output × 1ch (extensible to RGB888 with using option I/O)
  - ITU RBT-656 video capture × 1ch (extensible to RGB666 with using option I/O)
- USB 2.0 host (HS/FS protocols) × 1ch
- IDE66 (ATA/ATAPI-5) × 1ch
- SD memory interface (SDIO/CPRM: unsupported) × 1ch
- 10 bit A/D converter (1MS/s) × 2ch
- I^2C (I/O voltage: 3.3V) × 2ch
- UART × 3ch (extensible up to 6ch with using option I/O)
- 32/16 bit timer × 2ch
- DMAC × 8ch

Option I/O (with pin multiplex)

- RGB666 video output is extensible to 2ch
- Video capture is extensible to 2ch
- MediaLB (MOST50) × 1ch is addable
- CAN (I/O voltage: 3.3V) × 2ch is addable
- USB 2.0 function (HS/FS protocols) is switchable (USB 2.0 function and USB 2.0 host are accessed exclusively)
- GPIO is addable up to 24
- SPI × 1ch is addable
- PWM × 2ch is addable

- I2S is addable up to 3ch
- The number of UART channel is extensible up to 6ch
- The data width in the external bus interface is extensible to 32 bit

3. Block diagram

Figure 3-1 shows block diagram of MB86R01.

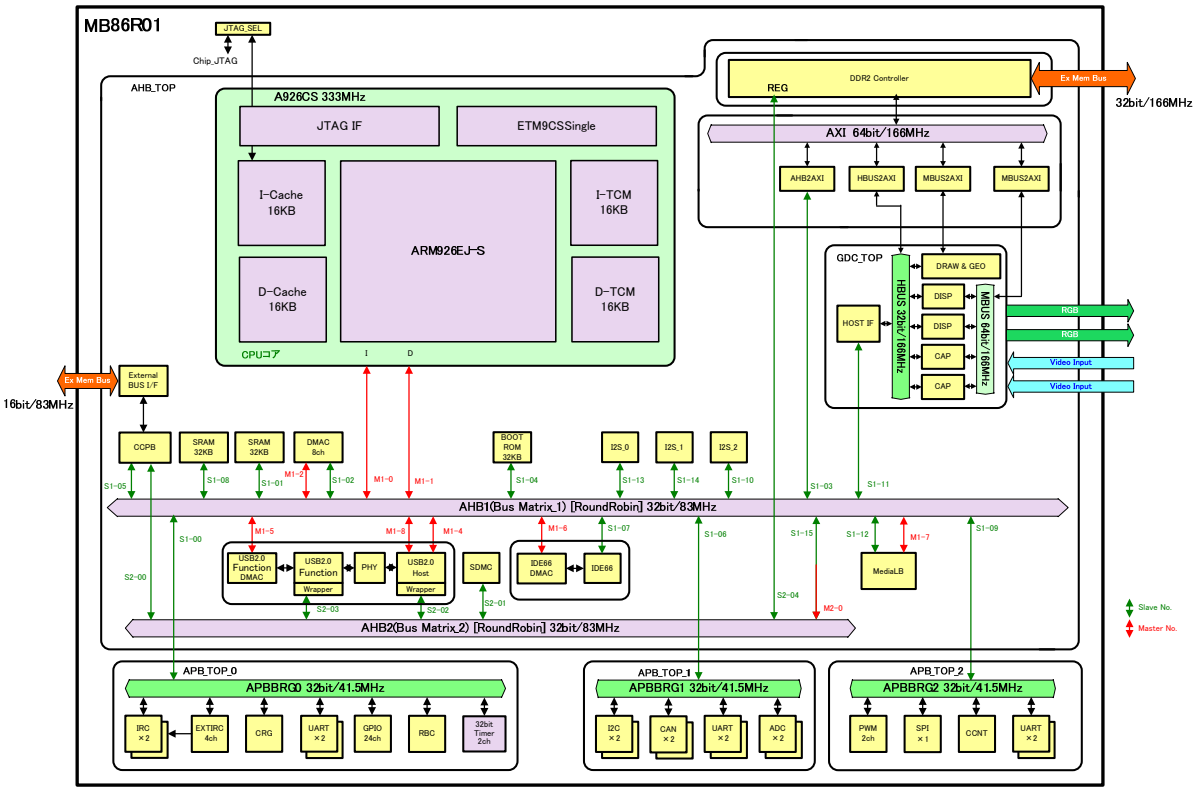


Figure 3-1 Block diagram of MB86R01

CPU core

This is CPU core block of ARM926EJ-S which is connected to each I/O through AHB bus in LSI. Instruction (I)/Data (D) function as a separate bus master for Harvard architecture.

GDC_TOP

This is MB86296 compatible GDC which has 2 functions: AHB slave function writes required display list for drawing to GDC with having CPU or DMA controller as master, and AXI master function reads display list arranged in DDR2 memory with having GDC as master.

AXI bus

This bus bridges main memory and internal resource. Following four bus masters are connected.

- AHB1: Each bus master of AHB bus such as CPU and DMA controller
- HBUS: HOST IF on GDC
- DRAW & GEO: Draw (2D/3D drawing) and GEO (geometry engine) on GDC
- MBUS: DISP (display controller) and CAP (Video capture) on GDC

AHB1 bus

Following resources are connected.

- CPU core: Bus masters of instruction (I)/data (D)
- GDC: GDC register part
- AHB2AXI: AXI port for main memory access
- CCPB: Encrypted ROM decoding block
- External BUS I/F: External bus interface (connected through CCPB)
- SRAM: General purpose internal SRAM 32KB × 2
- DMAC: General purpose DMA × 8ch
  It operates as bus master at data transfer
- Boot ROM: Built-in boot ROM
- I2S_0/1/2: Serial audio controller × 3ch
- USB 2.0 Function DMAC: USB function DMAC
  It operates as bus master at data transfer
- USB2.0 Host: It operates as USB2.0 EHCI, USB1.1 OHCI bus masters
- IDE66/IDE66DMAC: Register part of IDE host controller and built-in DMAC
  The DMAC part operates as bus master at data transfer
- MLB: MediaLB controller
- AHB2
- APBBRG0/1/2: AHB-APB bridge circuit × 3ch

AHB2 bus

- CCPB: Encrypted ROM decoding block
- USB 2.0 Function: USB 2.0 function controller's register part
- USB 2.0 Host: USB 2.0 host controller's register part
- SDMC: SD memory controller
- DDR2 controller: DDR2 controller's register part

APB_TOP_0

This block bridges between APBBRG0 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- Interrupt controller (IRC) × 2ch
- External interrupt controller (EXTIRC)
- Clock reset generator (CRG)
- UART (ch0 and ch1) × 2ch
- Remap boot controller (RBC)
- 32 bit general-purpose timer (32 bit timer) × 2ch

APB_TOP_1

This block bridges between APBBRG1 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- I^2C controller × 2ch
- CAN controller × 2ch
- UART (ch2 and ch3) × 2ch
- A/D converter (ADC) × 2ch

APB_TOP_2

This block bridges between APBBRG2 bus and AHB1 bus, and following low-speed peripheral resources are connected.

- PWM controller (PWM)
- SPI controller (SPI)
- CCNT
- UART (ch4 and ch5) × 2ch

4. Function list

Function list of MB86R01 is shown below.

Function	Outline
CPU core	• ARM926EJ-S™ processor core • Core operation frequency: 333MHz • 16KB instruction cache • 16KB data cache • Tightly-Coupled memory for 16KB instruction (ITCM) • Tightly-Coupled memory for 16KB data (DTCM) • ETM9CS Single and JTAG ICE debugging interface • Java acceleration (Jazelle technology)
Bus architecture	• Multilayer AHB bus architecture (software interrupt) • Speeding up data transfer between main memory and each bus master with 64 bit AXI bus
Interrupt	• High-speed interrupt × 1ch h (soft interrupt) • Normal interrupt × 64ch (external interrupt × 4ch + built-in internal interrupt × 60ch) • Up to 16 interrupt levels are settable by channel
Clock	• PLL multiplication: selectable from ×15 ~ 49 • Operation frequency: 333MHz (CPU), 83MHz (AHB), 41.5MHz (APB) • Low power consumption mode (clock to ARM and module is stoppable)
Reset	• Hardware reset, software reset, and watchdog reset
Remap	• ROM area is able to be mapping to built-in SRAM area
External bus interface	• Three chip select signals • Provided 32M byte address space in each chip select • Supported 16/32 bit width SRAM/Flash ROM connection • Programmable weight controller • Encrypted ROM compound engine
DDR2 controller	• Supported DDR2SDRAM (DDR2-400) • Connectable capacity: 256 ~ 512M bit × 2 or 256 ~ 512M bit × 1 • I/O width: Selectable from ×16/×32 bit • Max. transfer rate: 166MHz/333Mbps
Built-in SRAM	• Mounted general purpose SRAM of 32KB × 2 (32 bit bus)
DMAC	• AHB connection × 8ch • Transfer mode: Block, burst, and demand
Timer	• 32/16 bit programmable × 2 channels
GPIO (*2)	• Max. 24 is usable • Interrupt function
PWM (*2)	• Built-in 2 channels • Duty ratio and phase are configurable
A/D converter	• 10 bit successive approximation type A/D converter × 2ch • Sampling rate: 648KS/s (max. sampling plate) • Nonlinearity error: ± 2.0LSB (max.)

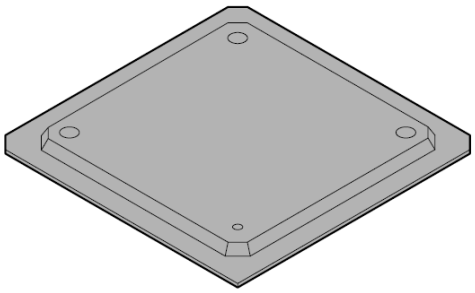
Function	Outline
GDC (*1)	• Display controller RGB666 or RGB888 output Max. resolution is 1024 × 768 Max. 6 layered display Max. 2 screen output • Digital video capture function BT.601, BT.656, and RGB666 Max. 2 inputs • Geometry engine (MB86296 compatible display list is usable) • 2D/3D drawing function (MB86296 compatible display list is usable)
I2S (*2)	• Audio output × 3ch (L/R)/Audio input × 3ch (L/R) • Supported three-wire serial (I2S, MSB-Justified) and serial PCM data transfer interface • Master/Slave operations are selectable • Resolution capability: Max. 32 bit/sample
UART (*2)	• Max. 6 channels (dedicated channel: 3ch, option: 3ch) • 1 channel: capable of input/output CTS/RTS signals • 8 bit pre-scaler for baud rate clock generation • Enabled DMA transfer
I^2C	• 3.3V pin × 2ch • Supported standard mode (max. 100kbps)/high-speed mode (max. 400kbps)
SPI (*2)	• Full duplex/Synchronous transmission • Transfer data length: 1 bit unit (max. 32 bit) (programmable setting)
CAN (*2)	• Mounted BOSCH C_CAN module × 2ch • Conformed to CAN protocol version 2.0 part A and B • I/O voltage: 3.3V
MediaLB (*2)	• 16 channels • MediaLB clock speed: 256Fs/512Fs/1024Fs • Built-in 9K bit channel buffer
USB (*2)	• USB 2.0 compliant Host/Function controller × 1ch (pin multiplex) • HS/FS protocol support (supported VBus and isochronous transfer)
IDE (*2)	• Supported ATA/ATAPI-5 • Equipped 1 channel • Supported primary IDE channel • Equipped transmission FIFO buffer (512 byte × 2) and reception FIFO buffer (512 byte × 2) for the ultra DMA transfer • Unsupported single word DMA and multiword DMA
SDMC	• Conformed to SD memory card physical layer specification 1.0 • Equipped 1 channel • Supported SD memory card and multimedia card • Unsupported SPI mode, SDIO mode, and CPRM
CCNT	• Mode selection of multiplex pin group 2 and 4 • Software reset control • AXI interconnection control (priority and WAIT setting)
JTAG	• Conformed to IEIEEE1149.1 (IEEE Standard Test Access Port and Boundary-Scan Architecture) • Supported JTAG ICE connection

*1: Number of layer of simultaneous display and number of output display as well as capture input for displaying in high resolution may be restricted due to data supply capacity of graphics memory (DDR2 controller).
*2: A part of external pin functions of this LSI is multiplexed. Max. number of usable channel is limited by pin multiplex function setting.

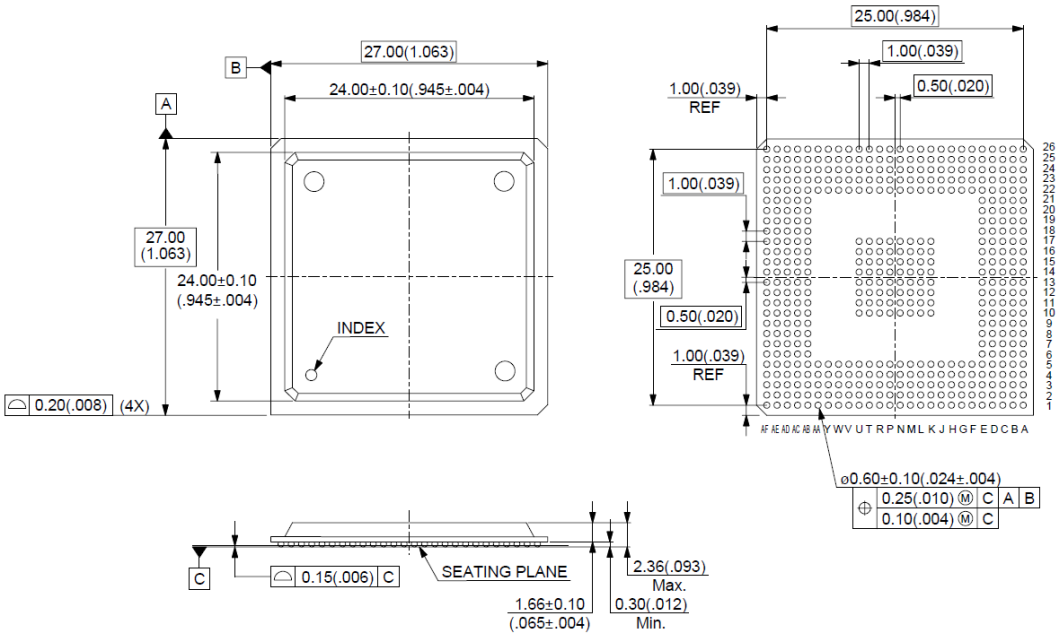
5. Package dimension

Package dimension of MB86R01 is shown below.

BGA-484P-M07

484-pin plastic PBGA		
 (BGA-484P-M07)	Ball pitch	1.00 mm
	Package width × package length	27.00 mm × 27.00 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	2.36 mm Max

484-pin plastic PBGA
(BGA-484P-M07)

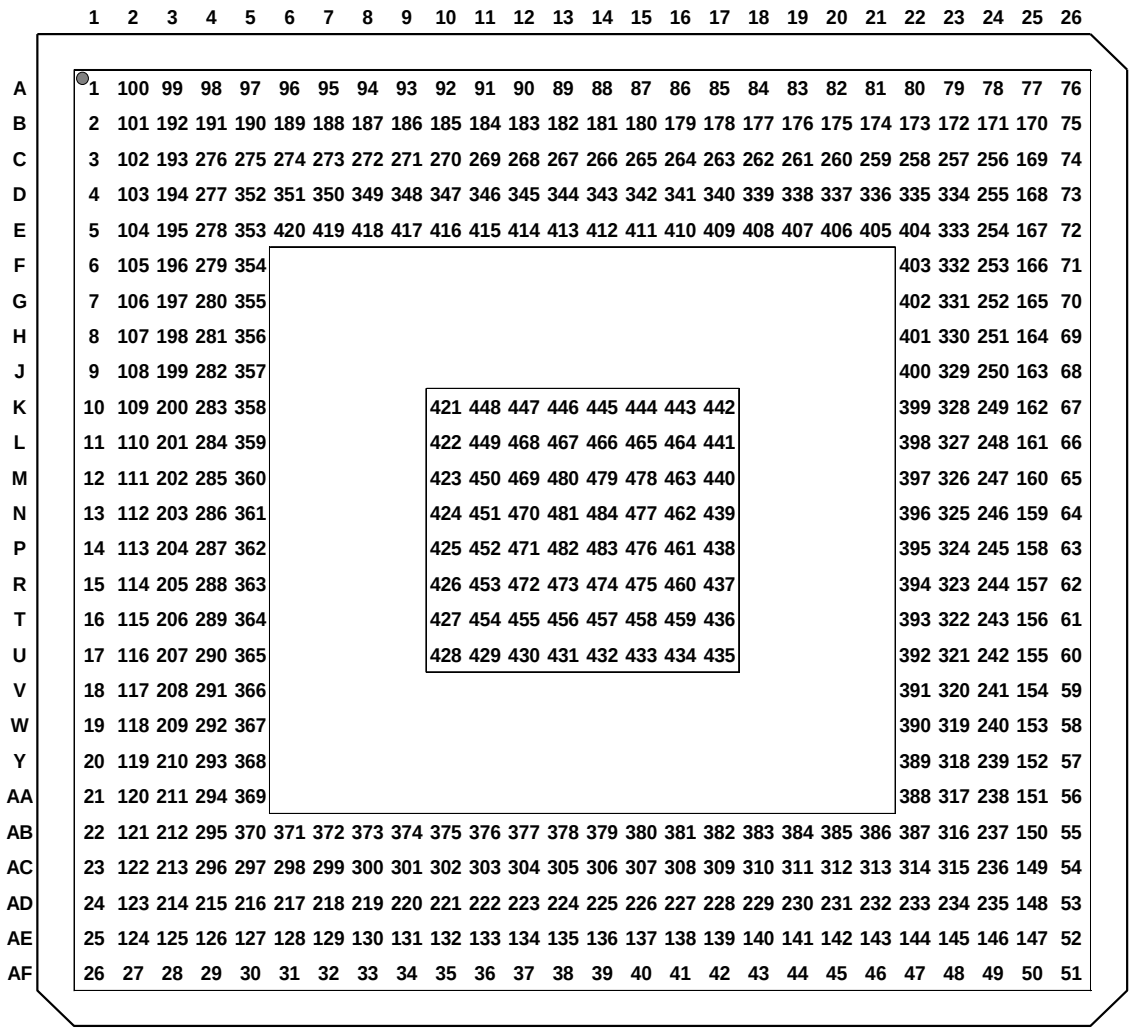


Dimensions in mm (inches).
Note: The values in parentheses are reference values.

6. Pin assignment

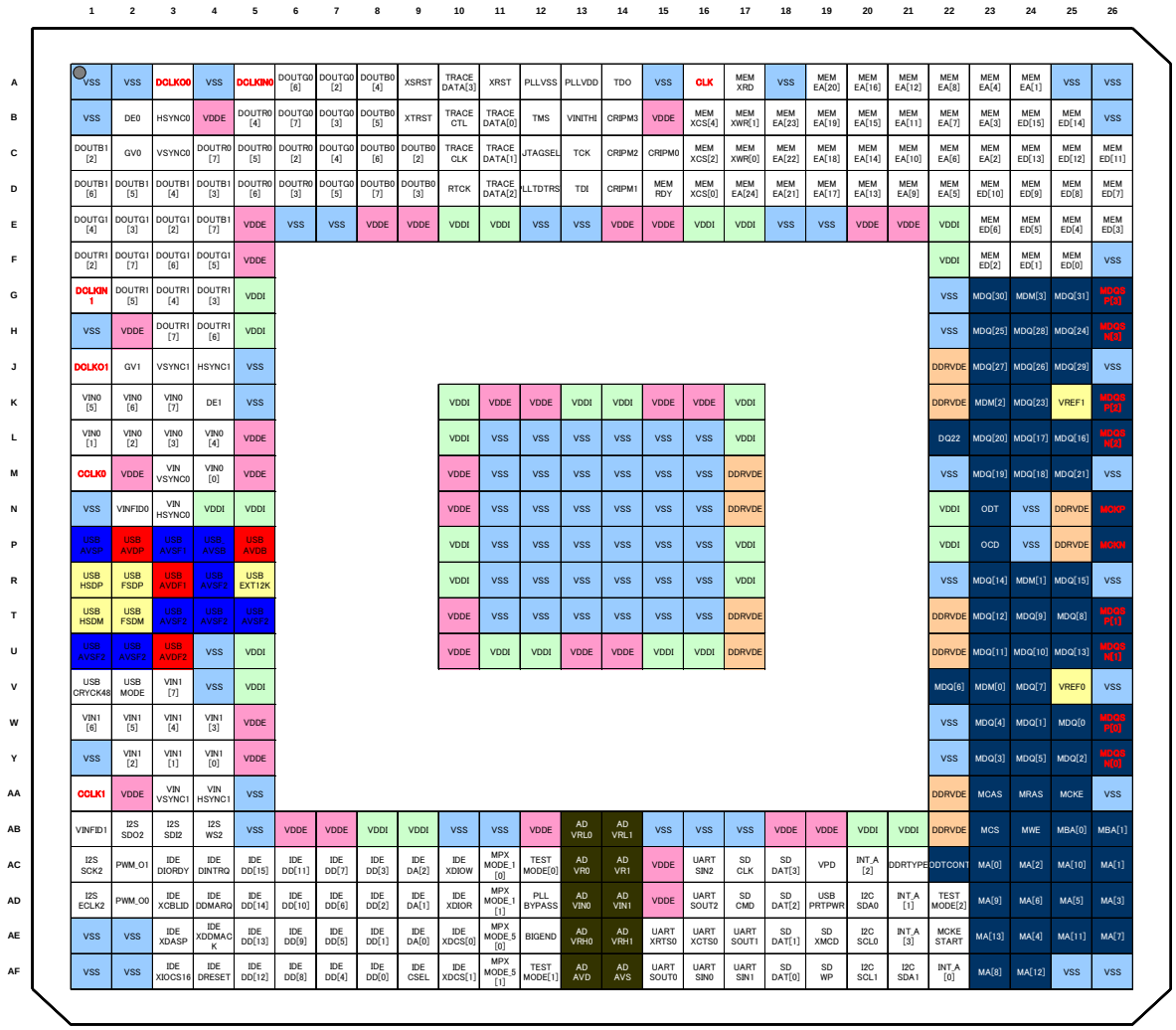
Pin assignment of MB86R01 is shown below.

(Top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	1	100	99	98	97	96	95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80	79	78	77	76
B	2	101	192	191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	174	173	172	171	170	75
C	3	102	193	276	275	274	273	272	271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256	169	74
D	4	103	194	277	352	351	350	349	348	347	346	345	344	343	342	341	340	339	338	337	336	335	334	255	168	73
E	5	104	195	278	353	420	419	418	417	416	415	414	413	412	411	410	409	408	407	406	405	404	333	254	167	72
F	6	105	196	279	354																	403	332	253	166	71
G	7	106	197	280	355																	402	331	252	165	70
H	8	107	198	281	356																	401	330	251	164	69
J	9	108	199	282	357																	400	329	250	163	68
K	10	109	200	283	358						421	448	447	446	445	444	443	442				399	328	249	162	67
L	11	110	201	284	359						422	449	468	467	466	465	464	441				398	327	248	161	66
M	12	111	202	285	360						423	450	469	480	479	478	463	440				397	326	247	160	65
N	13	112	203	286	361						424	451	470	481	484	477	462	439				396	325	246	159	64
P	14	113	204	287	362						425	452	471	482	483	476	461	438				395	324	245	158	63
R	15	114	205	288	363						426	453	472	473	474	475	460	437				394	323	244	157	62
T	16	115	206	289	364						427	454	455	456	457	458	459	436				393	322	243	156	61
U	17	116	207	290	365						428	429	430	431	432	433	434	435				392	321	242	155	60
V	18	117	208	291	366																	391	320	241	154	59
W	19	118	209	292	367																	390	319	240	153	58
Y	20	119	210	293	368																	389	318	239	152	57
AA	21	120	211	294	369																	388	317	238	151	56
AB	22	121	212	295	370	371	372	373	374	375	376	377	378	379	380	381	382	383	384	385	386	387	316	237	150	55
AC	23	122	213	296	297	298	299	300	301	302	303	304	305	306	307	308	309	310	311	312	313	314	315	236	149	54
AD	24	123	214	215	216	217	218	219	220	221	222	223	224	225	226	227	228	229	230	231	232	233	234	235	148	53
AE	25	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	52
AF	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51

(Top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
A	VSS	VSS	DCLKO0	VSS	DCLKIN0	DOUTG0 [6]	DOUTG0 [2]	DOUTB0 [4]	XSRST	TRACE DATA[3]	XRST	PLLVSS	PLLVDD	TDO	VSS	CLK	MEM XRD	VSS	MEM EA[20]	MEM EA[16]	MEM EA[12]	MEM EA[8]	MEM EA[4]	MEM EA[1]	VSS	VSS
B	VSS	DE0	HSYNC0	VDDE	DOUTR0 [4]	DOUTG0 [7]	DOUTG0 [3]	DOUTB0 [5]	XTRST	TRACE CTL	TRACE DATA[0]	TMS	VINITHI	CRIPM3	VDDE	MEM XCS[4]	MEM XWR[1]	MEM EA[23]	MEM EA[19]	MEM EA[15]	MEM EA[11]	MEM EA[7]	MEM EA[3]	MEM ED[15]	MEM ED[14]	VSS
C	DOUTB1 [2]	GV0	VSYNC0	DOUTR0 [7]	DOUTR0 [5]	DOUTR0 [2]	DOUTG0 [4]	DOUTB0 [6]	DOUTB0 [2]	TRACE CLK	TRACE DATA[1]	JTAGSEL	TCK	CRIPM2	CRIPM0	MEM XCS[2]	MEM XWR[0]	MEM EA[22]	MEM EA[18]	MEM EA[14]	MEM EA[10]	MEM EA[6]	MEM EA[2]	MEM ED[13]	MEM ED[12]	MEM ED[11]
D	DOUTB1 [6]	DOUTB1 [5]	DOUTB1 [4]	DOUTB1 [3]	DOUTR0 [6]	DOUTR0 [3]	DOUTG0 [5]	DOUTB0 [7]	DOUTB0 [3]	RTCK	TRACE DATA[2]	TLLTDTRS	TDI	CRIPM1	MEM RDY	MEM XCS[0]	MEM EA[24]	MEM EA[21]	MEM EA[17]	MEM EA[13]	MEM EA[9]	MEM EA[5]	MEM ED[10]	MEM ED[9]	MEM ED[8]	MEM ED[7]
E	DOUTG1 [4]	DOUTG1 [3]	DOUTG1 [2]	DOUTB1 [7]	VDDE	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	VDDE	VDDI	MEM ED[6]	MEM ED[5]	MEM ED[4]	MEM ED[3]
F	DOUTR1 [2]	DOUTG1 [7]	DOUTG1 [6]	DOUTG1 [5]	VDDE																	VDDI	MEM ED[2]	MEM ED[1]	MEM ED[0]	VSS
G	DCLKIN 1	DOUTR1 [5]	DOUTR1 [4]	DOUTR1 [3]	VDDI																	VSS	MDQ[30]	MDM[3]	MDQ[31]	MDQS P[3]
H	VSS	VDDE	DOUTR1 [7]	DOUTR1 [6]	VDDI																	VSS	MDQ[25]	MDQ[28]	MDQ[24]	MDQS N[3]
J	DCLKO1	GV1	VSYNC1	HSYNC1	VSS																	DDRVDE	MDQ[27]	MDQ[26]	MDQ[29]	VSS
K	VIN0 [5]	VIN0 [6]	VIN0 [7]	DE1	VSS					VDDI	VDDE	VDDE	VDDI	VDDI	VDDE	VDDE	VDDI					DDRVDE	MDM[2]	MDQ[23]	VREF1	MDQS P[2]
L	VIN0 [1]	VIN0 [2]	VIN0 [3]	VIN0 [4]	VDDE					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					DQ22	MDQ[20]	MDQ[17]	MDQ[16]	MDQS N[2]
M	CCLK0	VDDE	VIN VSYNC0	VIN0 [0]	VDDE					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VSS	MDQ[19]	MDQ[18]	MDQ[21]	VSS
N	VSS	VINFID0	VIN HSYNC0	VDDI	VDDI					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					VDDI	ODT	VSS	DDRVDE	MCKP
P	USB AVSP	USB AVDP	USB AVSF1	USB AVSF	USB AVDF					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VDDI	OCD	VSS	DDRVDE	MCKN
R	USB HSDP	USB FSDP	USB AVDF1	USB AVSF2	USB EXT12K					VDDI	VSS	VSS	VSS	VSS	VSS	VSS	VDDI					VSS	MDQ[14]	MDM[1]	MDQ[15]	VSS
T	USB HSDM	USB FSDM	USB AVSF2	USB AVSF2	USB AVSF2					VDDE	VSS	VSS	VSS	VSS	VSS	VSS	DDRVDE					DDRVDE	MDQ[12]	MDQ[9]	MDQ[8]	MDQS P[1]
U	USB AVSF2	USB AVSF2	USB AVDF2	VSS	VDDI					VDDE	VDDI	VDDI	VDDE	VDDE	VDDI	VDDI	DDRVDE					DDRVDE	MDQ[11]	MDQ[10]	MDQ[13]	MDQS N[1]
V	USB CRYCK48	USB MODE	VIN1 [7]	VSS	VDDI																	MDQ[6]	MDM[0]	MDQ[7]	VREF0	VSS
W	VIN1 [6]	VIN1 [5]	VIN1 [4]	VIN1 [3]	VDDE																	VSS	MDQ[4]	MDQ[1]	MDQ[0	MDQS P[0]
Y	VSS	VIN1 [2]	VIN1 [1]	VIN1 [0]	VDDE																	VSS	MDQ[3]	MDQ[5]	MDQ[2]	MDQS N[0]
AA	CCLK1	VDDE	VIN VSYNC1	VIN HSYNC1	VSS																	DDRVDE	MCAS	MRAS	MCKE	VSS
AB	VINFID1	I2S SDO2	I2S SDI2	I2S WS2	VSS	VDDE	VDDE	VDDI	VDDI	VSS	VSS	VDDE	AD VRL0	AD VRL1	VSS	VSS	VSS	VDDE	VDDE	VDDI	VDDI	DDRVDE	MCS	MWE	MBA[0]	MBA[1]
AC	I2S SCK2	PWM_O1	IDE DIORDY	IDE DINTRQ	IDE DD[15]	IDE DD[11]	IDE DD[7]	IDE DD[3]	IDE DA[2]	IDE XDIOW	MPX MODE_1 [0]	TEST MODE[0]	AD VR0	AD VR1	VDDE	UART SIN2	SD CLK	SD DAT[3]	VPD	INT_A [2]	DDRTYPE	ODTCONT	MA[0]	MA[2]	MA[10]	MA[1]
AD	I2S ECLK2	PWM_O0	IDE XCBLID	IDE DDMARQ	IDE DD[14]	IDE DD[10]	IDE DD[6]	IDE DD[2]	IDE DA[1]	IDE XDIOR	MPX MODE_1 [1]	PLL BYPASS	AD VIN0	AD VIN1	VDDE	UART SOUT2	SD CMD	SD DAT[2]	USB PRTPWR	I2C SDA0	INT_A [1]	TEST MODE[2]	MA[9]	MA[6]	MA[5]	MA[3]
AE	VSS	VSS	IDE XDASP	IDE XDDMACK	IDE DD[13]	IDE DD[9]	IDE DD[5]	IDE DD[1]	IDE DA[0]	IDE XDCS[0]	MPX MODE_5 [0]	BIGEND	AD VRH0	AD VRH1	UART XRTS0	UART XCTS0	UART SOUT1	SD DAT[1]	SD XMCD	I2C SCL0	INT_A [3]	MCKE START	MA[13]	MA[4]	MA[11]	MA[7]
AF	VSS	VSS	IDE XIOCS16	IDE DRESET	IDE DD[12]	IDE DD[8]	IDE DD[4]	IDE DD[0]	IDE CSEL	IDE XDCS[1]	MPX MODE_5 [1]	TEST MODE[1]	AD AVD	AD AVS	UART SOUT0	UART SIN0	UART SIN1	SD DAT[0]	SD WP	I2C SCL1	I2C SDA1	INT_A [0]	MA[8]	MA[12]	VSS	VSS

Pin assignment table

Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME	Pin NO	JEDEC	PIN NAME
1	A1	VSS	101	B2	DE0	201	L3	VIN0[3]	301	AC9	IDE_DA[2]	401	H22	VSS
2	B1	VSS	102	C2	GV0	202	M3	VINVSYNC0	302	AC10	IDE_XDIOW	402	G22	VSS
3	C1	DOUTB1[2]	103	D2	DOUTB1[5]	203	N3	VINHSYNC0	303	AC11	MPX_MODE_1[0]	403	F22	VDDI
4	D1	DOUTB1[6]	104	E2	DOUTG1[3]	204	P3	USB_AVSF1	304	AC12	TESTMODE[0]	404	E22	VDDI
5	E1	DOUTG1[4]	105	F2	DOUTG1[7]	205	R3	USB_AVDF1	305	AC13	AD_VR0	405	E21	VDDE
6	F1	DOUTR1[2]	106	G2	DOUTR1[5]	206	T3	USB_AVSF2	306	AC14	AD_VR1	406	E20	VDDE
7	G1	DCLKIN1	107	H2	VDDE	207	U3	USB_AVDF2	307	AC15	VDDE	407	E19	VSS
8	H1	VSS	108	J2	GV1	208	V3	VIN1[7]	308	AC16	UART_SIN2	408	E18	VSS
9	J1	DCLKO1	109	K2	VIN0[6]	209	W3	VIN1[4]	309	AC17	SD_CLK	409	E17	VDDI
10	K1	VIN0[5]	110	L2	VIN0[2]	210	Y3	VIN1[1]	310	AC18	SD_DAT[3]	410	E16	VDDI
11	L1	VIN0[1]	111	M2	VDDE	211	AA3	VINVSYNC1	311	AC19	VPD	411	E15	VDDE
12	M1	CCLK0	112	N2	VINFID0	212	AB3	I2S_SDI2	312	AC20	INT_A[2]	412	E14	VDDE
13	N1	VSS	113	P2	USB_AVDP	213	AC3	IDE_DIORDY	313	AC21	DDRTYPE	413	E13	VSS
14	P1	USB_AVSP	114	R2	USB_FSDP	214	AD3	IDE_XCBLID	314	AC22	ODTCONT	414	E12	VSS
15	R1	USB_HSDP	115	T2	USB_FSDM	215	AD4	IDE_DDMARQ	315	AC23	MA[0]	415	E11	VDDI
16	T1	USB_HSDM	116	U2	USB_AVSF2	216	AD5	IDE_DD[14]	316	AB23	MCS	416	E10	VDDI
17	U1	USB_AVSF2	117	V2	USB_MODE	217	AD6	IDE_DD[10]	317	AA23	MCAS	417	E9	VDDE
18	V1	USB_CRYCK48	118	W2	VIN1[5]	218	AD7	IDE_DD[6]	318	Y23	MDQ[3]	418	E8	VDDE
19	W1	VIN1[6]	119	Y2	VIN1[2]	219	AD8	IDE_DD[2]	319	W23	MDQ[4]	419	E7	VSS
20	Y1	VSS	120	AA2	VDDE	220	AD9	IDE_DA[1]	320	V23	MDM[0]	420	E6	VSS
21	AA1	CCLK1	121	AB2	I2S_SDO2	221	AD10	IDE_XDIOR	321	U23	MDQ[11]	421	K10	VDDI
22	AB1	VINFID1	122	AC2	PWM_O1	222	AD11	MPX_MODE_1[1]	322	T23	MDQ[12]	422	L10	VDDI
23	AC1	I2S_SCK2	123	AD2	PWM_O0	223	AD12	PLLBYPASS	323	R23	MDQ[14]	423	M10	VDDE
24	AD1	I2S_ECLK2	124	AE2	VSS	224	AD13	AD_VIN0	324	P23	OCD	424	N10	VDDE
25	AE1	VSS	125	AE3	IDE_XDASP	225	AD14	AD_VIN1	325	N23	ODT	425	P10	VDDI
26	AF1	VSS	126	AE4	IDE_XDDMACK	226	AD15	VDDE	326	M23	MDQ[19]	426	R10	VDDI
27	AF2	VSS	127	AE5	IDE_DD[13]	227	AD16	UART_SOUT2	327	L23	MDQ[20]	427	T10	VDDE
28	AF3	IDE_XIOCS16	128	AE6	IDE_DD[9]	228	AD17	SD_CMD	328	K23	MDM[2]	428	U10	VDDE
29	AF4	IDE_XDRESET	129	AE7	IDE_DD[5]	229	AD18	SD_DAT[2]	329	J23	MDQ[27]	429	U11	VDDI
30	AF5	IDE_DD[12]	130	AE8	IDE_DD[1]	230	AD19	USB_PRTPWR	330	H23	MDQ[25]	430	U12	VDDI
31	AF6	IDE_DD[8]	131	AE9	IDE_DA[0]	231	AD20	I2C_SDA0	331	G23	MDQ[30]	431	U13	VDDE
32	AF7	IDE_DD[4]	132	AE10	IDE_XDCS[0]	232	AD21	INT_A[1]	332	F23	MEM_ED[2]	432	U14	VDDE
33	AF8	IDE_DD[0]	133	AE11	MPX_MODE_5[0]	233	AD22	TESTMODE[2]	333	E23	MEM_ED[6]	433	U15	VDDI
34	AF9	IDE_CSEL	134	AE12	BIGEND	234	AD23	MA[9]	334	D23	MEM_ED[10]	434	U16	VDDI
35	AF10	IDE_XDCS[1]	135	AE13	AD_VRH0	235	AD24	MA[6]	335	D22	MEM_EA[5]	435	U17	DDRVDE
36	AF11	MPX_MODE_5[1]	136	AE14	AD_VRH1	236	AC24	MA[2]	336	D21	MEM_EA[9]	436	T17	DDRVDE
37	AF12	TESTMODE[1]	137	AE15	UART_XRTS0	237	AB24	MWE	337	D20	MEM_EA[13]	437	R17	VDDI
38	AF13	AD_AVD	138	AE16	UART_XCTS0	238	AA24	MRAS	338	D19	MEM_EA[17]	438	P17	VDDI
39	AF14	AD_AVS	139	AE17	UART_SOUT1	239	Y24	MDQ[5]	339	D18	MEM_EA[21]	439	N17	DDRVDE
40	AF15	UART_SOUT0	140	AE18	SD_DAT[1]	240	W24	MDQ[1]	340	D17	MEM_EA[24]	440	M17	DDRVDE
41	AF16	UART_SIN0	141	AE19	SD_XMCD	241	V24	MDQ[7]	341	D16	MEM_XCS[0]	441	L17	VDDI
42	AF17	UART_SIN1	142	AE20	I2C_SCL0	242	U24	MDQ[10]	342	D15	MEM_RDY	442	K17	VDDI
43	AF18	SD_DAT[0]	143	AE21	INT_A[3]	243	T24	MDQ[9]	343	D14	CRIPM1	443	K16	VDDE
44	AF19	SD_WP	144	AE22	MCKE_START	244	R24	MDM[1]	344	D13	TDI	444	K15	VDDE
45	AF20	I2C_SCL1	145	AE23	MA[13]	245	P24	VSS	345	D12	PLLTDTRST	445	K14	VDDI
46	AF21	I2C_SDA1	146	AE24	MA[4]	246	N24	VSS	346	D11	TRACEDATA[2]	446	K13	VDDI
47	AF22	INT_A[0]	147	AE25	MA[11]	247	M24	MDQ[18]	347	D10	RTCK	447	K12	VDDE
48	AF23	MA[8]	148	AD25	MA[5]	248	L24	MDQ[17]	348	D9	DOUTB0[3]	448	K11	VDDE
49	AF24	MA[12]	149	AC25	MA[10]	249	K24	MDQ[23]	349	D8	DOUTB0[7]	449	L11	VSS
50	AF25	VSS	150	AB25	MBA[0]	250	J24	MDQ[26]	350	D7	DOUTG0[5]	450	M11	VSS
51	AF26	VSS	151	AA25	MCKE	251	H24	MDQ[28]	351	D6	DOUTR0[3]	451	N11	VSS
52	AE26	MA[7]	152	Y25	MDQ[2]	252	G24	MDM[3]	352	D5	DOUTR0[6]	452	P11	VSS
53	AD26	MA[3]	153	W25	MDQ[0]	253	F24	MEM_ED[1]	353	E5	VDDE	453	R11	VSS
54	AC26	MA[1]	154	V25	VREF0	254	E24	MEM_ED[5]	354	F5	VDDE	454	T11	VSS
55	AB26	MBA[1]	155	U25	MDQ[13]	255	D24	MEM_ED[9]	355	G5	VDDI	455	T12	VSS
56	AA26	VSS	156	T25	MDQ[8]	256	C24	MEM_ED[13]	356	H5	VDDI	456	T13	VSS
57	Y26	MDQSN[0]	157	R25	MDQ[15]	257	C23	MEM_EA[2]	357	J5	VSS	457	T14	VSS
58	W26	MDQSP[0]	158	P25	DDRVDE	258	C22	MEM_EA[6]	358	K5	VSS	458	T15	VSS
59	V26	VSS	159	N25	DDRVDE	259	C21	MEM_EA[10]	359	L5	VDDE	459	T16	VSS
60	U26	MDQSN[1]	160	M25	MDQ[21]	260	C20	MEM_EA[14]	360	M5	VDDE	460	R16	VSS
61	T26	MDQSP[1]	161	L25	MDQ[16]	261	C19	MEM_EA[18]	361	N5	VDDI	461	P16	VSS
62	R26	VSS	162	K25	VREF1	262	C18	MEM_EA[22]	362	P5	USB_AVDB	462	N16	VSS
63	P26	MCKN	163	J25	MDQ[29]	263	C17	MEM_XWR[0]	363	R5	USB_EXT12K	463	M16	VSS
64	N26	MCKP	164	H25	MDQ[24]	264	C16	MEM_XCS[2]	364	T5	USB_AVSF2	464	L16	VSS
65	M26	VSS	165	G25	MDQ[31]	265	C15	CRIPM0	365	U5	VDDI	465	L15	VSS
66	L26	MDQSN[2]	166	F25	MEM_ED[0]	266	C14	CRIPM2	366	V5	VDDI	466	L14	VSS
67	K26	MDQSP[2]	167	E25	MEM_ED[4]	267	C13	TCK	367	W5	VDDE	467	L13	VSS
68	J26	VSS	168	D25	MEM_ED[8]	268	C12	JTAGSEL	368	Y5	VDDE	468	L12	VSS
69	H26	MDQSN[3]	169	C25	MEM_ED[12]	269	C11	TRACEDATA[1]	369	AA5	VSS	469	M12	VSS
70	G26	MDQSP[3]	170	B25	MEM_ED[14]	270	C10	TRACECLK	370	AB5	VSS	470	N12	VSS
71	F26	VSS	171	B24	MEM_ED[15]	271	C9	DOUTB0[2]	371	AB6	VDDE	471	P12	VSS
72	E26	MEM_ED[3]	172	B23	MEM_EA[3]	272	C8	DOUTB0[6]	372	AB7	VDDE	472	R12	VSS
73	D26	MEM_ED[7]	173	B22	MEM_EA[7]	273	C7	DOUTG0[4]	373	AB8	VDDI	473	R13	VSS
74	C26	MEM_ED[11]	174	B21	MEM_EA[11]	274	C6	DOUTR0[2]	374	AB9	VDDI	474	R14	VSS
75	B26	VSS	175	B20	MEM_EA[15]	275	C5	DOUTR0[5]	375	AB10	VSS	475	R15	VSS
76	A26	VSS	176	B19	MEM_EA[19]	276	C4	DOUTR0[7]	376	AB11	VSS	476	P15	VSS
77	A25	VSS	177	B18	MEM_EA[23]	277	D4	DOUTB1[3]	377	AB12	VDDE	477	N15	VSS
78	A24	MEM_EA[1]	178	B17	MEM_XWR[1]	278	E4	DOUTB1[7]	378	AB13	AD_VRL0	478	M15	VSS
79	A23	MEM_EA[4]	179	B16	MEM_XCS[4]	279	F4	DOUTG1[5]	379	AB14	AD_VRL1	479	M14	VSS
80	A22	MEM_EA[8]	180	B15	VDDE	280	G4	DOUTR1[3]	380	AB15	VSS	480	M13	VSS
81	A21	MEM_EA[12]	181	B14	CRIPM3	281	H4	DOUTR1[6]	381	AB16	VSS	481	N13	VSS
82	A20	MEM_EA[16]	182	B13	VINITHI	282	J4	HSYNC1	382	AB17	VSS	482	P13	VSS
83	A19	MEM_EA[20]	183	B12	TMS	283	K4	DE1	383	AB18	VDDE	483	P14	VSS
84	A18	VSS	184	B11	TRACEDATA[0]	284	L4	VIN0[4]	384	AB19	VDDE	484	N14	VSS
85	A17	MEM_XRD	185	B10	TRACECTL	285	M4	VIN0[0]	385	AB20	VDDI			
86	A16	CLK	186	B9	XTRST	286	N4	VDDI	386	AB21	VDDI			
87	A15	VSS	187	B8	DOUTB0[5]	287	P4	USB_AVSB	387	AB22	DDRVDE			
88	A14	TDO	188	B7	DOUTG0[3]	288	R4	USB_AVSF2	388	AA22	DDRVDE			
89	A13	PLLVDD	189	B6	DOUTG0[7]	289	T4	USB_AVSF2	389	Y22	VSS			
90	A12	PLLVSS	190	B5	DOUTR0[4]	290	U4	VSS	390	W22	VSS			
91	A11	XRST	191	B4	VDDE	291	V4	VSS	391	V22	MDQ[6]			
92	A10	TRACEDATA[3]	192	B3	HSYNC0	292	W4	VIN1[3]	392	U22	DDRVDE			
93	A9	XSRST	193	C3	VSYNC0	293	Y4	VIN1[0]	393	T22	DDRVDE			
94	A8	DOUTB0[4]	194	D3	DOUTB1[4]	294	AA4	VINHSYNC1	394	R22	VSS			
95	A7	DOUTG0[2]	195	E3	DOUTG1[2]	295	AB4	I2S_WS2	395	P22	VDDI			
96	A6	DOUTG0[6]	196	F3	DOUTG1[6]	296	AC4	IDE_DINTRQ	396	N22	VDDI			
97	A5	DCLKIN0	197	G3	DOUTR1[4]	297	AC5	IDE_DD[15]	397	M22	VSS			
98	A4	VSS	198	H3	DOUTR1[7]	298	AC6	IDE_DD[11]	398	L22	MDQ[22]			
99	A3	DCLKO0	199	J3	VSYNC1	299	AC7	IDE_DD[7]	399	K22	DDRVDE			
100	A2	VSS	200	K3	VIN0[7]	300	AC8	IDE_DD[3]	400	J22	DDRVDE			

7. Pin function

External pin function of MB86R01 is described below.

7.1. Pin Multiplex

This LSI adopts pin multiplex function, and a part of external pin function is multiplexed.
The external pin function is categorized into following five groups. Each group is able to set the external pin function individually; therefore, the function can be flexibly set depending on the peripheral I/O resource to be used.

1. Pin multiplex group #1 (setting pin: MPX_MODE_1[1:0])
   - Mode 0: Pin related to DISPLAY1
   - Mode 1: Pin related to external bus interface
   - Mode 2: Pin related to I2S0, GPIO, and DISPLAY0 data width extension
2. Pin multiplex group #2 (setting register: CMUX_MD.MPX_MODE_2[2:0])
   - Mode 0: Pin related to CAP1, CAP0 synchronizing signal, PWM, and I2S2
   - Mode 1: Pin related to CAP1 (NRGB666)
   - Mode 2: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2
   - Mode 3: Pin related to GPIO, CAN, I2S1, MediaLB, and SPI
   - Mode 4: Pin related to GPIO, CAN, I2S1, MediaLB, and I2S2 (input)
3. Pin multiplex group #3 (setting pin: USB_MODE)
   - Mode 0: Pin related to USB 2.0 host
   - Mode 1: Pin related to USB 2.0 function
4. Pin multiplex group #4 (setting register: CMUX_MD.MPX_MODE_4[1:0])
   - Mode 0: Pin related to IDE
   - Mode 1: Pin related to I2S1, CAN, GPIO, and PWM
5. Pin multiplex group #5 (setting pin: MPX_MODE_5[1:0])
   - Mode 0: Pin related to ETM
   - Mode 1: Pin related to UART3, UART4, and UART5
   - Mode 2: Pin related to UART3, UART4, and PWM

Note:
Mode should be changed when each pin is not in operation.
PWM, I2S1, and CAN pins may be duplicated and allocated to external pin depending on group combination; in this case, use either of them. For unused pin, follow the procedure in 1.6.27, unused pin with pin multiplex function in the duplex case.

Pin multiplex group #1 (setting pin: MPX_MODE_1 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1	Mode 2			
		Pin related to DISPLAY1	Pin related to external bus interface	Pin related to I2S0	Pin related to GPIO	Pin related to DISPLAY0	Pin related to external bus interface
198	H3	DOUTR1[7]	MEM_ED[31]	I2S_ECLK0	-	-	-
281	H4	DOUTR1[6]	MEM_ED[30]	I2S_SCK0	-	-	-
106	G2	DOUTR1[5]	MEM_ED[29]	I2S_WS0	-	-	-
197	G3	DOUTR1[4]	MEM_ED[28]	I2S_SDI0	-	-	-
280	G4	DOUTR1[3]	MEM_ED[27]	I2S_SDO0	-	-	-
6	F1	DOUTR1[2]	MEM_ED[26]	-	GPIO_PD[12]	-	-
105	F2	DOUTG1[7]	MEM_ED[25]	-	GPIO_PD[11]	-	-
196	F3	DOUTG1[6]	MEM_ED[24]	-	GPIO_PD[10]	-	-
279	F4	DOUTG1[5]	MEM_ED[23]	-	GPIO_PD[9]	-	-
5	E1	DOUTG1[4]	MEM_ED[22]	-	GPIO_PD[8]	-	-
104	E2	DOUTG1[3]	MEM_ED[21]	-	GPIO_PD[7]	-	-
195	E3	DOUTG1[2]	MEM_ED[20]	-	GPIO_PD[6]	-	-
278	E4	DOUTB1[7]	MEM_ED[19]	-	-	DOUTR0[1]	-
4	D1	DOUTB1[6]	MEM_ED[18]	-	-	DOUTR0[0]	-
103	D2	DOUTB1[5]	MEM_ED[17]	-	-	DOUTG0[1]	-
194	D3	DOUTB1[4]	MEM_ED[16]	-	-	DOUTG0[0]	-
277	D4	DOUTB1[3]	MEM_XWR[3]	-	-	DOUTB0[1]	-
3	C1	DOUTB1[2]	MEM_XWR[2]	-	-	DOUTB0[0]	-
283	K4	DE1	XDACK[7]	-	-	-	XDACK[7]
282	J4	HSYNC1	DREQ[6]	-	-	-	DREQ[6]
199	J3	VSYNC1	XDACK[6]	-	-	-	XDACK[6]
108	J2	GV1	DREQ[7]	-	-	-	DREQ[7]

Pin multiplex group #1 mode setting

This mode is set with external pin, MPX_MODE_1[1:0].

MPX_MODE_1[1] pin	MPX_MODE_1[0] pin	Pin multiplex group #1 mode
"L"	"L"	Mode 0
"L"	"H"	Mode 1
"H"	"L"	Mode 2
"H"	"H"	Mode 0

Pin multiplex group #2 (setting register: PIN MPX Select.MPX_MODE_2 [2:0])

Pin No.	JEDEC	Mode0			Mode1	Mode2				Mode3					Mode4			
		Pin related to CAP0/1	Pin related to PWM	Pin related to I2S2	Pin related to CAP1 (NRGB666)	Pin related to GPIO	Pin related to CAN	Pin related to I2S1/2	Pin related to MediaLB	Pin related to GPIO	Pin related to CAN	Pin related to I2S1	Pin related to MediaLB	Pin related to SPI	Pin related to GPIO	Pin related to CAN	Pin related to I2S1/2	Pin related to MediaLB
208	V3	VIN1[7]	-	-	RI1[7]	GPIO_PD[5]	-	-	-	GPIO_PD[5]	-	-	-	-	GPIO_PD[5]	-	-	-
19	W1	VIN1[6]	-	-	RI1[6]	GPIO_PD[4]	-	-	-	GPIO_PD[4]	-	-	-	-	GPIO_PD[4]	-	-	-
118	W2	VIN1[5]	-	-	RI1[5]	-	CAN_TX0	-	-	-	CAN_TX0	-	-	-	-	CAN_TX0	-	-
209	W3	VIN1[4]	-	-	RI1[4]	-	CAN_RX0	-	-	-	CAN_RX0	-	-	-	-	CAN_RX0	-	-
292	W4	VIN1[3]	-	-	RI1[3]	-	CAN_TX1	-	-	-	CAN_TX1	-	-	-	-	CAN_TX1	-	-
119	Y2	VIN1[2]	-	-	RI1[2]	-	CAN_RX1	-	-	-	CAN_RX1	-	-	-	-	CAN_RX1	-	-
210	Y3	VIN1[1]	-	-	GI1[7]	-	-	I2S_SCK1	-	-	-	I2S_SCK1	-	-	-	-	I2S_SCK1	-
293	Y4	VIN1[0]	-	-	GI1[6]	-	-	I2S_WS1	-	-	-	I2S_WS1	-	-	-	-	I2S_WS1	-
211	AA3	VINVSYNC1	-	-	VINVSYNC1	-	-	I2S_ECLK1	-	-	-	I2S_ECLK1	-	-	-	-	I2S_ECLK1	-
294	AA4	VINHSYNC1	-	-	VINHSYNC1	-	-	I2S_SDI1	-	-	-	I2S_SDI1	-	-	-	-	I2S_SDI1	-
22	AB1	VINFID1	-	-	VINFID1	-	-	I2S_SDO1	-	-	-	I2S_SDO1	-	-	-	-	I2S_SDO1	-
202	M3	VINVSYNC0	-	-	GI1[5]	-	-	-	MLB_DATA	-	-	-	MLB_DATA	-	-	-	-	MLB_DATA
203	N3	VINHSYNC0	-	-	GI1[4]	-	-	-	MLB_SIG	-	-	-	MLB_SIG	-	-	-	-	MLB_SIG
112	N2	VINFID0	-	-	GI1[3]	-	-	-	MLB_CLK	-	-	-	MLB_CLK	-	-	-	-	MLB_CLK
123	AD2	-	PWM_O0	-	GI1[2]	GPIO_PD[3]	-	-	-	GPIO_PD[3]	-	-	-	-	GPIO_PD[3]	-	-	-
122	AC2	-	PWM_O1	-	BI1[7]	GPIO_PD[2]	-	-	-	GPIO_PD[2]	-	-	-	-	GPIO_PD[2]	-	-	-
121	AB2	-	-	I2S_SDO2	BI1[6]	-	-	I2S_SDO2	-	-	-	-	-	SPI_DO	GPIO_PD[1]	-	-	-
24	AD1	-	-	I2S_ECLK2	BI1[5]	-	-	I2S_ECLK2	-	-	-	-	-	Reserved (Input/Output)	GPIO_PD[0]	-	-	-
23	AC1	-	-	I2S_SCK2	BI1[4]	-	-	I2S_SCK2	-	-	-	-	-	SPI_SCK	-	-	I2S_SCK2	-
295	AB4	-	-	I2S_WS2	BI1[3]	-	-	I2S_WS2	-	-	-	-	-	SPI_SS	-	-	I2S_WS2	-
212	AB3	-	-	I2S_SDI2	BI1[2]	-	-	I2S_SDI2	-	-	-	-	-	SPI_DI	-	-	I2S_SDI2	-

Pin multiplex group #2 mode setting

This mode is set with MPX_MODE_2 bit (bit 2-0) in the multiplex mode setting register (CMUX_MD.)

MPX_MODE_2 (bit 2-0) of the CMUX_MD register	Pin multiplex group #2 mode
000	Mode 0
001	Mode 1
010	Mode 2
011	Mode 3
100	Mode 4
101 – 0110	Reserved
111	(Initial value)

Pin multiplex group #3 (setting pin: USB_MODE)

Pin No.	JEDEC	Mode 0	Mode 1
		Pin related to USB 2.0 host	Pin related to USB 2.0 function
114	R2	USB_FSDP	USB_FSDP
115	T2	USB_FSDM	USB_FSDM
15	R1	USB_HSDP	USB_HSDP
16	T1	USB_HSDM	USB_HSDM
18	V1	USB_CRYCK48	USB_CRYCK48
230	AD19	USB_PRTPWR	USB_PRTPWR

Pin multiplex group #3 mode setting

This mode is set with external pin, USB_MODE.

USB_MODE pin	Pin multiplex group #3 mode
"L"	Mode 0
"H"	Mode 1

Pin multiplex group #4 (setting register: PIN_MPX_Select.MPX_MODE_4 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1				
		Pin related to IDE	Pin related to I2S1	Pin related to CAN	Pin related to GPIO	Pin related to PWM	Unused pin (input/output)
29	AF4	IDE_XDRESET	-	-	-	-	Reserved (output)
28	AF3	IDE_XIOCS16	I2S_SDI1	-	-	-	-
125	AE3	IDE_XDASP	I2S_WS1	-	-	-	-
215	AD4	IDE_DDMARQ	I2S_ECLK1	-	-	-	-
296	AC4	IDE_DINTRQ	I2S_SDO1	-	-	-	-
214	AD3	IDE_XCBLID	I2S_SCK1	-	-	-	-
297	AC5	IDE_DD[15]	-	CAN_TX0	-	-	-
216	AD5	IDE_DD[14]	-	CAN_RX0	-	-	-
127	AE5	IDE_DD[13]	-	CAN_TX1	-	-	-
30	AF5	IDE_DD[12]	-	CAN_RX1	-	-	-
298	AC6	IDE_DD[11]	-	-	GPIO_PD[23]	-	-
217	AD6	IDE_DD[10]	-	-	GPIO_PD[22]	-	-
128	AE6	IDE_DD[9]	-	-	GPIO_PD[21]	-	-
31	AF6	IDE_DD[8]	-	-	GPIO_PD[20]	-	-
299	AC7	IDE_DD[7]	-	-	GPIO_PD[19]	-	-
218	AD7	IDE_DD[6]	-	-	GPIO_PD[18]	-	-
129	AE7	IDE_DD[5]	-	-	GPIO_PD[17]	-	-
32	AF7	IDE_DD[4]	-	-	GPIO_PD[16]	-	-
300	AC8	IDE_DD[3]	-	-	GPIO_PD[15]	-	-
219	AD8	IDE_DD[2]	-	-	GPIO_PD[14]	-	-
130	AE8	IDE_DD[1]	-	-	GPIO_PD[13]	-	-
33	AF8	IDE_DD[0]	-	-	-	-	Reserved (input/output)
213	AC3	IDE_DIORDY	-	-	-	-	Reserved (input)
301	AC9	IDE_DA[2]	-	-	-	-	Reserved (output)
220	AD9	IDE_DA[1]	-	-	-	PWM_O1	-
131	AE9	IDE_DA[0]	-	-	-	PWM_O0	-
35	AF10	IDE_XDCS[1]	-	-	-	-	Reserved (output)
132	AE10	IDE_XDCS[0]	-	-	-	-	Reserved (output)
221	AD10	IDE_XDIOR	-	-	-	-	Reserved (output)
302	AC10	IDE_XDIOW	-	-	-	-	Reserved (output)
34	AF9	IDE_CSEL	-	-	-	-	Reserved (output)
126	AE4	IDE_XDDMACK	-	-	-	-	Reserved (output)

Pin multiplex group #4 mode setting

This mode is set with MPX_MODE_4 bit (bit 5-4) in the multiplex mode setting register (CMUX_MD.)

MPX_MODE_4 (Bit 5-4) of the CMUX_MD register	Pin multiplex group #4 mode
00	Mode 0
01	Mode 1
10	Reserved
11	(Initial value)

Pin multiplex group #5 (setting pin: MPX_MODE_5 [1:0])

Pin No.	JEDEC	Mode 0	Mode 1	Mode 2	
		Pin related to ETM	Pin related to UART3/4/5	Pin related to UART3/4	Pin related to PWM
270	C10	TRACECLK	UART_SIN3	UART_SIN3	-
185	B10	TRACECTL	UART_SOUT3	UART_SOUT3	-
92	A10	TRACEDATA[3]	UART_SIN4	UART_SIN4	-
346	D11	TRACEDATA[2]	UART_SOUT4	UART_SOUT4	-
269	C11	TRACEDATA[1]	UART_SIN5	-	PWM_O1
184	B11	TRACEDATA[0]	UART_SOUT5	-	PWM_O0

Pin multiplex group #5 mode setting

This mode is set with external pin, MPX_MODE_5[1:0].

MPX_MODE_5[1] pin	MPX_MODE_5[0] pin	Pin multiplex group #5 mode
"L"	"L"	Mode 0
"L"	"H"	Mode 1
"H"	"L"	Mode 2
"H"	"H"	Mode 0

7.2. Pin Function

Format

Pin function list is shown in the following format.

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description

Meaning of item and sign

Pin name

Name of external pin.

I/O

Input/Output signal's distinction based on this LSI.

- I: Pin that can be used as input
- O: Pin that can be used as output
- IO: Pin that can be used as input and output (interactive pin)

Polarity

Active polarity of external pin's input/output signals

- P: "H" active pin (positive logic)
- N: "L" active pin (negative logic)
- PN: "H" and "L" active pins

Analog/Digital

Signal type of external pin

- A: Analog signal
- D: Digital signal

Type

Input/Output circuit type of external pin.

- CLK:
- POD: Pseudo Open Drain
- PU: Pull Up
- PD: Pull Down
- ST: Schmitt Type
- Tri: Tri-state

Pin status after reset

Pin status after external pin reset

- H: "H" level
- L: "L" level
- HiZ: High impedance
- X: "H" level or "L" level
- A: Clock output

Description

Outline of external pin function

7.2.1. External bus interface related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
MEM_XCS[4]	O	N	D	-	H	Chip select 4
MEM_XCS[2]	O	N	D	-	H	Chip select 2
MEM_XCS[0]	O	N	D	-	H	Chip select 0
MEM_XRD	O	N	D	-	H	Read strobe
MEM_XWR[3:2]	O	N	D	-	H	Write strobe MEM_XWR[3] -> MEM_ED[31:24], MEM_XWR[2] -> MEM_ED[23:16] (optional pin)
MEM_XWR[1:0]	O	N	D	-	H	Write strobe MEM_XWR[1] -> MEM_ED[15:8], MEM_XWR[0] -> MEM_ED[7:0]
MEM_RDY	I	P	D	-	-	Ready input for slow device
MEM_EA[24:1]	O	-	D	-	L	Address bus
MEM_ED[31:16]	IO	-	D	-	HiZ	Bi-directional data bus (optional pin)
MEM_ED[15:0]	IO	-	D	-	HiZ	Bi-directional data Bus
DREQ[7:6]	I	-	D	-	-	External DMA request
XDACK[7:6]	O	P	D	-	L	External DMA acknowledge

7.2.2. IDE66 related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
IDE_XDRESET	O	N	D	-	H	IDE reset
IDE_DD[15:0]	IO	-	D	PD	L	IDE device data
IDE_XDCS[1:0]	O	N	D	-	H	IDE chip select
IDE_DA[2:0]	O	P	D	-	L	IDE device address
IDE_XDIOR	O	N	D	-	H	IDE device I/O read
IDE_XDIOW	O	N	D	-	H	IDE device I/O write
IDE_DIORDY	I	P	D	-	-	IDE I/O channel ready
IDE_DDMARQ	I	P	D	-	-	IDE device DMA request
IDE_XDDMACK	O	N	D	-	H	IDE device DMA acknowledge
IDE_CSEL	O	P	D	-	L	IDE cable select
IDE_XIOCS16	I	N	D	-	-	IDE 16 bit I/O
IDE_XDASP	I	N	D	PD	-	IDE device active
IDE_DINTRQ	I	P	D	PD	-	IDE Interrupt
IDE_XCBLID	I	N	D	PD	-	IDE cable ID

7.2.3. SD Memory controller related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
SD_CLK	O	N	D	-	L	Media clock
SD_CMD	IO	-	D	-	HiZ	Media command
SD_DAT[3:0]	IO	-	D	-	HiZ	Media data
SD_WP	I	P	D	-	-	Media write protection
SD_XMCD	I	N	D	-	-	Media card detection

7.2.4. USB 2.0 Host/Function related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
USB_FSDP	IO	-	A	-	-	D+ for FS
USB_FSDM	IO	-	A	-	-	D- for FS
USB_HSDP	IO	-	A	-	-	D+ for HS
USB_HSDM	IO	-	A	-	-	D- for HS
USB_CRYCK48	I	-	D	CLK	-	Clock used for USB communication
USB_PRTPWR	O	-	D	-	L	USB port power control
USB_EXT12K	O	-	A	-	-	External resistance pin This should be connected to USB_AVDB through 12kΩ resistance.
USB_AVSP	I	-	A	-	-	PLL ground
USB_AVSB	I	-	A	-	-	Reference voltage ground
USB_AVDP	I	-	A	-	-	PLL power supply
USB_AVDB	I	-	A	-	-	Reference voltage power supply
USB_AVSF1	I	-	A	-	-	Driver/Receiver ground 1
USB_AVDF1	I	-	A	-	-	Driver/Receiver power supply 1
USB_AVSF2	I	-	A	-	-	Driver/Receiver ground 2
USB_AVDF2	I	-	A	-	-	Driver/Receiver power supply 2

7.2.5. External interrupt controller related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
INT_A[3:0]	I	PN	D	-	-	Asynchronous external interrupt requests

7.2.6. UART related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
UART_SIN0	I	P	D	-	-	Input data signal
UART_SOUT0	O	P	D	-	H	Output data signal
UART_XCTS0	I	N	D	-	-	Clear to send
UART_XRTS0	O	N	D	-	H	Request to send
UART_SIN1	I	P	D	-	-	Input data signal
UART_SOUT1	O	P	D	-	H	Output data signal
UART_SIN2	I	P	D	-	-	Input data signal
UART_SOUT2	O	P	D	-	H	Output data signal
UART_SIN3	I	P	D	-	-	Input data signal (optional)
UART_SOUT3	O	P	D	-	H	Output data signal (optional)
UART_SIN4	I	P	D	-	-	Input data signal (optional)
UART_SOUT4	O	P	D	-	H	Output data signal (optional)
UART_SIN5	I	P	D	-	-	Input data signal (optional)
UART_SOUT5	O	P	D	-	H	Output data signal (optional)

7.2.7. CAN related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
CAN_TX0	O	-	D	PD	H	Transmission (optional)
CAN_RX0	I	-	D	PD	-	Reception (optional)
CAN_TX1	O	-	D	PD	H	Transmission (optional)
CAN_RX1	I	-	D	PD	-	Reception (optional)

7.2.8. I2S related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
I2S_ECLK0	I	-	D	-	-	External clock (optional)
I2S_SCK0	IO	-	D	-	HiZ	Clock (optional)
I2S_WS0	IO	PN	D	-	HiZ	Sync (optional)
I2S_SDI0	I	P	D	-	-	Input data signal (optional)
I2S_SDO0	O	P	D	-	Hiz	Output data signal (optional)
I2S_ECLK1	I	-	D	-	-	External clock (optional)
I2S_SCK1	IO	-	D	PD	L	Clock (optional)
I2S_WS1	IO	PN	D	PD	L	Sync(optional)
I2S_SDI1	I	P	D	-	-	Input data signal (optional)
I2S_SDO1	O	P	D	PD	L	Output data signal (optional)
I2S_ECLK2	I	-	D	PD	-	External clock (optional)
I2S_SCK2	IO	-	D	PD	L	Clock (optional)
I2S_WS2	IO	PN	D	PD	L	Sync (optional)
I2S_SDI2	I	P	D	-	-	Input data signal (optional)
I2S_SDO2	O	P	D	PD	L	Output data signal (optional)

7.2.9. I^2C related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
I2C_SCL0	IO	-	D	POD	HiZ	I2C clock
I2C_SDA0	IO	-	D	POD	HiZ	I2C data
I2C_SCL1	IO	-	D	POD	HiZ	I2C clock
I2C_SDA1	IO	-	D	POD	HiZ	I2C data

7.2.10. SPI related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
SPI_DO	O	P	D	PD	L	Serial data output (optional)
SPI_DI	I	P	D	-	-	Serial data input (optional)
SPI_SCK	O	-	D	PD	L	Serial clock (optional)
SPI_SS	O	PN	D	PD	L	Slave select (optional)

7.2.11. PWM related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
PWM_O0	O	-	D	PD (*1)	L	PWM out 0 (optional)
PWM_O1	O	-	D	PD (*1)	L	PWM out 1 (optional)

*1: Only PWM pin of the pin multiplex group #2 is with pull-down resistance.

7.2.12. A/D converter related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
AD_VIN0	I	-	A	-	-	A/D analog input
AD_VRH0	I	-	A	-	-	Reference voltage "H" input
AD_VRL0	I	-	A	-	-	Reference voltage "L" input
AD_AVD	I	-	A	-	-	Analog power supply
AD_VR0	O	-	A	-	-	Reference output
AD_VIN1	I	-	A	-	-	A/D analog input
AD_VRH1	I	-	A	-	-	Reference voltage "H" input
AD_VRL1	I	-	A	-	-	Reference voltage "L" input
AD_AVS	I	-	A	-	-	Analog ground
AD_VR1	O	-	A	-	-	Reference output

7.2.13. DDR2 related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
MA[13:0]	O	P	D	-	H	Address
MBA[1:0]	O	P	D	-	H	Bank address
MDQ[31:0]	IO	P	D	-	H	Data (*5)
MDM[3:0]	O	P	D	-	HiZ	Data mask (*6)
MDQSP[3:0]	IO	P	D	-	HiZ	Data strobe (*5)
MDQSN[3:0]	IO	N	D	-	HiZ	Data strobe (*5)
MCKP	O	P	D	CLK	L	Clock output
MCKN	O	N	D	CLK	H	Clock output
MCKE	O	P	D	-	L	Clock enable
MCS	O	N	D	-	L	Chip select
MRAS	O	N	D	-	H	Row address strobe
MCAS	O	N	D	-	H	Column address strobe
MWE	O	N	D	-	H	Write enable
DDRVDE	I	-	A	-	-	SSTL_18 1.8V power supply
VREF1	I	-	A	-	-	Reference voltage input (DDRVDE/2)
VREF0	I	-	A	-	-	Reference voltage input (DDRVDE/2)
OCD	O	-	A	-	-	Off chip driver reference voltage input (*1)
ODT	O	-	A	-	-	On-die termination reference voltage input (*2)
ODTCONT	O	P	D	-	L	On-die termination control (*3)
MCKE_START	I	P	D	-	-	Set a state of MCKE in reset 0: Low (*4) 1: High (reserved)
DDRTYPE	I	P	D	-	-	Pull-up pin to VDDE via high resistance

*1: Pull up the pin to DDRVDE (1.8V power supply), via 200Ω resistance
*2: PCB impedance Z = 100Ω or 50Ω: Pull up pin to DDRVDE (1.8V power supply), via a 180Ω resistance.
PCB impedance Z = 150Ω or 75Ω: Pull up pin to DDRVDE (1.8V power supply), via a 240Ω resistance.
*3: It connects it with the ODT pin of DDR2SDRAM
*4: Pull down pin to VSS, via high resistance
*5: This is process of unused pin at 16 bit mode. Pull down the pin to VSS via high resistance.
Unused pins at 16 bit mode are as follows:
"MDQ[31:16], MDQSP[3:2], MDQSN[3:2]"
*6: This is process of MDM[3:2] at 16 bit mode. Be sure to open this pin.

7.2.14. DISPLAY related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Explanation
HSYNC0	IO	-	D	-	HiZ	Video output interface horizontal sync output Horizontal sync input in external sync mode
VSYNC0	IO	-	D	-	HiZ	Video output interface vertical sync output Vertical sync input in external sync mode
GV0	O	-	D	-	L	Video output interface graphics/video switch
DCLKIN0	I	-	D	CLK	-	Video output interface dot clock input
DCLKO0	O	-	D	CLK	X	Video output interface dot clock output
DE0	O	-	D	-	X	DE/CSYNC
DOUTR0[7:2]	O	-	D	-	X	Digital RGB output0 DataR[7:2]
DOUTR0[1:0]	O	-	D	-	X	Digital RGB output0 DataR[1:0] (optional)
DOUTG0[7:2]	O	-	D	-	X	Digital RGB output0 DataG[7:2]
DOUTG0[1:0]	O	-	D	-	X	Digital RGB output0 DataG[1:0] (optional)
DOUTB0[7:2]	O	-	D	-	X	Digital RGB output0 DataB[7:2]
DOUTB0[1:0]	O	-	D	-	X	Digital RGB output0 DataB[1:0] (optional)
HSYNC1	IO	-	D	-	HiZ	Video output interface horizontal sync output Horizontal sync input in external sync mode
VSYNC1	IO	-	D	-	HiZ	Video output interface vertical sync output Vertical sync input in external sync mode
GV1	O	-	D	-	L	Video output interface graphics/video switch
DCLKIN1	I	-	D	CLK	-	Video output interface dot clock input
DCLKO1	O	-	D	CLK	X	Video output interface dot clock output
DE1	O	-	D	-	X	DE/CSYNC
DOUTR1[7:2]	O	-	D	-	X	Digital RGB output1 DataR[7:2]
DOUTG1[7:2]	O	-	D	-	X	Digital RGB output1 DataG[7:2]
DOUTB1[7:2]	O	-	D	-	X	Digital RGB output1 DataB[7:2]

Note:

When R:G:B = 5:5:5, lower 1 bit is set with the data contents of the upper 5 bits.

[Upper 5 bits]		[Lower 1 bit]
DOUTR0[7:3]=00000	->	DOUTR0[2]=0 (Low)
DOUTR0[7:3]=00001-11111	->	DOUTR0[2]=1 (High)
DOUTR1[7:3]=00000	->	DOUTR1[2]=0 (Low)
DOUTR1[7:3]=00001-11111	->	DOUTR1[2]=1 (High)

DOUTG0[7:2], DOUTG1[7:2], DOUTB0[7:2], and DOUTB1[7:2] have also the same spec.

7.2.15. Video capture related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
VIN0[7:0]	I	-	D	-	-	Video capture Data[7:0]
VINVSYNC0	I	-	D	PD	-	Video capture vertical sync input
VINHSYNC0	I	-	D	PD	-	Video capture horizontal sync input
VINFID0	I	-	D	-	-	Video input field identification signal 0 in odd field
CCLK0	I	-	D	CLK	-	Video capture input clock
VIN1[7:0]	I	-	D	PD	-	Video capture Data[7:0]
VINVSYNC1	I	-	D	-	-	Video capture vertical sync input
VINHSYNC1	I	-	D	-	-	Video capture horizontal sync input
VINFID1	I	-	D	PD	-	Video input field identification signal 0 in odd field
CCLK1	I	-	D	CLK	-	Video capture input clock
RI1[7:2]	I	-	D	PD	-	NRGB666 capture DataR[7:2] (optional)
GI1[7:2]	I	-	D	PD (*1)	-	NRGB666 capture DataG[7:2] (optional)
BI1[7:2]	I	-	D	PD (*2)	-	NRGB666 capture DataB[7:2] (optional)

*1: GI1[3] is not applicable.
*2: BI1[2] is not applicable.

7.2.16. System related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
CLK	I	-	D	CLK	-	Input clock
XRST	I	N	D	ST	-	System reset
CRIPM[3:0]	I	-	D	-	-	PLLMODE setting
VINITHI	I	-	D	-	-	Boot high address
PLLBYPASS	I	-	D	-	-	PLL bypass mode setting
BIGEND	I	-	D	-	-	LSI endian setting Low: Little endian High: Big endian
PLLVSS	I	-	A	-	-	PLL ground
PLLTDTRST	I	-	D	-	-	Test pin Pull up the pin to VDDE, via high resistance
PLLVDD	I	-	A	-	-	PLL power supply

7.2.17. JTAG related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
TCK	I	-	D	ST, PU	-	Test clock
XTRST	I	N	D	ST, PU	-	Test reset
TMS	I	N	D	PU	-	Test mode
TDI	I	-	D	PU	-	Test data input
TDO	O	-	D	Tri	HiZ	Test data output

7.2.18. ICE related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
RTCK	O	-	D	-	H	Return test clock
XSRST	IO	N	D	ST, PU	H	System reset

7.2.19. Multiplex setting related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
JTAGSEL	I	-	D	-	-	JTAG selection 1: DFT, 0: Normal Pull it down to VSS, via high resistance
MPX_MODE_5[1:0]	I	-	D	-	-	External pin multiplex mode 5
MPX_MODE_1[1:0]	I	-	D	-	-	External pin multiplex mode 1
USB_MODE	I	-	D	-	-	USB selection 0: Host, 1: Function
TESTMODE[2:0]	I	-	D	-	-	Test mode selection pin Pull it down to VSS, via high resistance
VPD	I	-	D	-	-	Test mode selection pin Pull it down to VSS, via high resistance

7.2.20. ETM related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
TRACECLK	O	-	D	-	L	Exported clock for TRACEDATA[3:0] and TRACECTL They are valid on bath edges of TRACECLK for max. integrity.
TRACECTL	O	-	D	-	H	Trace control signal used by the trace tool such as RealView supplied by ARM Limited.
TRACEDATA[3:0]	O	-	D	-	LHHH	Trace data used by the trace tool such as RealView supplied by ARM Limited.

7.2.21. Power supply related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
VSS	I	-	D	-	-	Ground
VDDE	I	-	D	-	-	External pin power supply
VDDI	I	-	D	-	-	Internal power supply

7.2.22. MediaLB related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
MLB_DATA	IO	P	D	PD	HiZ	Data (optional) (*1)
MLB_SIG	IO	P	D	PD	HiZ	Control (optional) (*1)
MLB_CLK	I	-	D	CLK	-	Clock (optional) (*1)

*1: MediaLB pin of this LSI uses 3.3[V] I/O; therefore, when connecting bus's voltage is not 3.3[V], level conversion at external side is needed.

7.2.23. GPIO related pin

Pin name	I/O	Polarity	Analog /Digital	Type	Status of pin after reset	Description
GPIO_PD[23:0]	IO	-	D	PD (*1)	HiZ	General purpose I/O port (optional)

*1: GPIO_PD[12:6] is not applicable.

7.2.24. Unused pin

Proceed following processes for unused pin.

Pin No.	JEDEC	Pin name	Process
3	C1	DOUTB1[2], MEM_XWR[2], DOUTB0[0]	Pull up to VDDE or pull down to VSS through high resistance.
4	D1	DOUTB1[6], MEM_ED[18], DOUTR0[0]	
5	E1	DOUTG1[4], MEM_ED[22], GPIO_PD[8]	
6	F1	DOUTR1[2], MEM_ED[26], GPIO_PD[12]	
7	G1	DCLKIN1	
9	J1	DCLKO1	Keep the pin open.
10	K1	VIN0[5]	Pull up to VDDE or pull down to VSS through high resistance.
11	L1	VIN0[1]	
12	M1	CCLK0	
14	P1	USB_AVSP	Connect to VSS.
15	R1	USB_HSDP	Pull down to VSS through 10kΩ resistance.
16	T1	USB_HSDM	
17	U1	USB_AVSF2	Connect to VSS.
18	V1	USB_CRYCK48	Pull up to VDDE or pull down to VSS through high resistance.
19	W1	VIN1[6], RI1[6], GPIO_PD[4]	Keep the pin open.
21	AA1	CCLK1	Pull up to VDDE or pull down to VSS through high resistance.
22	AB1	VINFID1, I2S_SDO1	Keep the pin open.
23	AC1	I2S_SCK2, BI1[4], SPI_SCK	
24	AD1	I2S_ECLK2, BI1[5], Reserved (input/output), GPIO_PD[0]	
28	AF3	IDE_XIOCS16, I2S_SDI1	Pull up to VDDE or pull down to VSS through high resistance.
29	AF4	IDE_XDRESET, Reserved (output)	Keep the pin open.
30	AF5	IDE_DD[12], CAN_RX1	
31	AF6	IDE_DD[8], GPIO_PD[20]	
32	AF7	IDE_DD[4], GPIO_PD[16]	
33	AF8	IDE_DD[0], Reserved (input/output)	
34	AF9	IDE_CSEL, Reserved (output)	
35	AF10	IDE_XDCS[1], Reserved (output)	
36	AF11	MPX_MODE_5[1]	Pull up to VDDE or pull down to VSS through high resistance.
38	AF13	AD_AVD	Connect to VSS.
39	AF14	AD_AVS	
40	AF15	UART_SOUT0	Keep the pin open.
41	AF16	UART_SIN0	Pull up to VDDE or pull down to VSS through high resistance.
42	AF17	UART_SIN1	
43	AF18	SD_DAT[0]	
44	AF19	SD_WP	

Pin No.	JEDEC	Pin name	Process
45	AF20	I2C_SCL1	Pull up to VDDE or pull down to VSS through high resistance.
46	AF21	I2C_SDA1	
47	AF22	INT_A[0]	
48	AF23	MA[8]	Keep the pin open.
49	AF24	MA[12]	
52	AE26	MA[7]	
53	AD26	MA[3]	
54	AC26	MA[1]	
55	AB26	MBA[1]	
57	Y26	MDQSN[0]	Pull down to VSS through high resistance.
58	W26	MDQSP[0]	
60	U26	MDQSN[1]	
61	T26	MDQSP[1]	
63	P26	MCKN	Keep the pin open.
64	N26	MCKP	
66	L26	MDQSN[2]	Pull down to VSS through high resistance.
67	K26	MDQSP[2]	
69	H26	MDQSN[3]	
70	G26	MDQSP[3]	
72	E26	MEM_ED[3]	Pull up to VDDE or pull down to VSS through high resistance.
73	D26	MEM_ED[7]	
74	C26	MEM_ED[11]	
78	A24	MEM_EA[1]	
79	A23	MEM_EA[4]	
80	A22	MEM_EA[8]	
81	A21	MEM_EA[12]	
82	A20	MEM_EA[16]	
83	A19	MEM_EA[20]	
85	A17	MEM_XRD	
88	A14	TDO	Keep the pin open.
92	A10	TRACEDATA[3], UART_SIN4	Pull up to VDDE or pull down to VSS through high resistance.
94	A8	DOUTB0[4]	Keep the pin open.
95	A7	DOUTG0[2]	
96	A6	DOUTG0[6]	
97	A5	DCLKIN0	Pull up to VDDE or pull down to VSS through high resistance.
99	A3	DCLKO0	Keep the pin open.
101	B2	DE0	
102	C2	GV0	
103	D2	DOUTB1[5], MEM_ED[17], DOUTG0[1]	Pull up to VDDE or pull down to VSS through high resistance.
104	E2	DOUTG1[3], MEM_ED[21], GPIO_PD[7]	
105	F2	DOUTG1[7], MEM_ED[25], GPIO_PD[11]	

Pin No.	JEDEC	Pin name	Process
106	G2	DOUTR1[5], MEM_ED[29], I2S_WS0	Pull up to VDDE or pull down to VSS through high resistance.
108	J2	GV1, DREQ[7]	
109	K2	VIN0[6]	
110	L2	VIN0[2]	
112	N2	VINFID0, GI1[3], MLB_CLK	
113	P2	USB_AVDP	Connect to VDDI.
114	R2	USB_FSDP	Pull down to VSS through 10kΩ resistance.
115	T2	USB_FSDM	
116	U2	USB_AVSF2	Connect to VSS.
117	V2	USB_MODE	Pull up to VDDE or pull down to VSS through high resistance.
118	W2	VIN1[5], RI1[5], CAN_TX0	Keep the pin open.
119	Y2	VIN1[2], RI1[2], CAN_RX1	
121	AB2	I2S_SDO2, BI1[6], SPI_DO, GPIO_PD[1]	
122	AC2	PWM_O1, BI1[7], GPIO_PD[2]	
123	AD2	PWM_O0, GI1[2], GPIO_PD[3]	
125	AE3	IDE_XDASP, I2S_WS1	
126	AE4	IDE_XDDMACK, Reserved (output)	
127	AE5	IDE_DD[13], CAN_TX1	
128	AE6	IDE_DD[9], GPIO_PD[21]	
129	AE7	IDE_DD[5], GPIO_PD[17]	
130	AE8	IDE_DD[1], GPIO_PD[13]	
131	AE9	IDE_DA[0], PWM_O0	
132	AE10	IDE_XDCS[0], Reserved (output)	
133	AE11	MPX_MODE_5[0]	Pull up to VDDE or pull down to VSS through high resistance.
135	AE13	AD_VRH0	Connect to VSS.
136	AE14	AD_VRH1	
137	AE15	UART_XRTS0	Keep the pin open.
138	AE16	UART_XCTS0	Pull up to VDDE or pull down to VSS through high resistance.
139	AE17	UART_SOUT1	Keep the pin open.
140	AE18	SD_DAT[1]	Pull up to VDDE or pull down to VSS through high resistance.
141	AE19	SD_XMCD	
142	AE20	I2C_SCL0	
143	AE21	INT_A[3]	
144	AE22	MCKE_START	Pull down to VSS through high resistance.
145	AE23	MA[13]	Keep the pin open.
146	AE24	MA[4]	
147	AE25	MA[11]	
148	AD25	MA[5]	
149	AC25	MA[10]	
150	AB25	MBA[0]	

Pin No.	JEDEC	Pin name	Process
151	AA25	MCKE	Keep the pin open.
152	Y25	MDQ[2]	Pull down to VSS through high resistance.
153	W25	MDQ[0]	
154	V25	VREF0	Connect to DDRVDE/2[V]Reference voltage.
155	U25	MDQ[13]	Pull down to VSS through high resistance.
156	T25	MDQ[8]	
157	R25	MDQ[15]	
160	M25	MDQ[21]	
161	L25	MDQ[16]	
162	K25	VREF1	Connect to DDRVDE/2[V]Reference voltage.
163	J25	MDQ[29]	Pull down to VSS through high resistance.
164	H25	MDQ[24]	
165	G25	MDQ[31]	
166	F25	MEM_ED[0]	Pull up to VDDE or pull down to VSS through high resistance.
167	E25	MEM_ED[4]	
168	D25	MEM_ED[8]	
169	C25	MEM_ED[12]	
170	B25	MEM_ED[14]	
171	B24	MEM_ED[15]	
172	B23	MEM_EA[3]	
173	B22	MEM_EA[7]	
174	B21	MEM_EA[11]	
175	B20	MEM_EA[15]	
176	B19	MEM_EA[19]	
177	B18	MEM_EA[23]	
178	B17	MEM_XWR[1]	
179	B16	MEM_XCS[4]	
183	B12	TMS	
184	B11	TRACEDATA[0], UART_SOUT5, PWM_O0	
185	B10	TRACECTL, UART_SOUT3	Keep the pin open.
187	B8	DOUTB0[5]	
188	B7	DOUTG0[3]	
189	B6	DOUTG0[7]	
190	B5	DOUTR0[4]	
192	B3	HSYNC0	Pull up to VDDE or pull down to VSS through high resistance.
193	C3	VSYNC0	
194	D3	DOUTB1[4], MEM_ED[16], DOUTG0[0]	
195	E3	DOUTG1[2], MEM_ED[20], GPIO_PD[6]	
196	F3	DOUTG1[6], MEM_ED[24], GPIO_PD[10]	
197	G3	DOUTR1[4], MEM_ED[28], I2S_SDI0	
198	H3	DOUTR1[7], MEM_ED[31], I2S_ECLK0	
199	J3	VSYNC1, XDACK[6]	

Pin No.	JEDEC	Pin name	Process
200	K3	VIN0[7]	Pull up to VDDE or pull down to VSS through high resistance.
201	L3	VIN0[3]	
202	M3	VINVSYNC0, GI1[5], MLB_DATA	Keep the pin open.
203	N3	VINHSYNC0, GI1[4], MLB_SIG	
204	P3	USB_AVSF1	Connect to VSS.
205	R3	USB_AVDF1	Connect to VDDE.
206	T3	USB_AVSF2	Connect to VSS.
207	U3	USB_AVDF2	Connect to VDDI.
208	V3	VIN1[7], RI1[7], GPIO_PD[5]	Keep the pin open.
209	W3	VIN1[4], RI1[4], CAN_RX0	
210	Y3	VIN1[1], GI1[7], I2S_SCK1	
211	AA3	VINVSYNC1, I2S_ECLK1	Pull up to VDDE or pull down to VSS through high resistance.
212	AB3	I2S_SDI2, BI1[2], SPI_DI	
213	AC3	IDE_DIORDY, Reserved (input)	
214	AD3	IDE_XCBLID, I2S_SCK1	Keep the pin open.
215	AD4	IDE_DDMARQ, I2S_ECLK1	Pull up to VDDE or pull down to VSS through high resistance.
216	AD5	IDE_DD[14], CAN_RX0	Keep the pin open.
217	AD6	IDE_DD[10], GPIO_PD[22]	
218	AD7	IDE_DD[6], GPIO_PD[18]	
219	AD8	IDE_DD[2], GPIO_PD[14]	
220	AD9	IDE_DA[1], PWM_O1	
221	AD10	IDE_XDIOR, Reserved (output)	
222	AD11	MPX_MODE_1[1]	Pull up to VDDE or pull down to VSS through high resistance.
224	AD13	AD_VIN0	Connect to VSS.
225	AD14	AD_VIN1	
227	AD16	UART_SOUT2	Keep the pin open.
228	AD17	SD_CMD	Pull up to VDDE or pull down to VSS through high resistance.
229	AD18	SD_DAT[2]	
230	AD19	USB_PRTPWR	Keep the pin open.
231	AD20	I2C_SDA0	Pull up to VDDE or pull down to VSS through high resistance.
232	AD21	INT_A[1]	
234	AD23	MA[9]	Keep the pin open.
235	AD24	MA[6]	
236	AC24	MA[2]	
237	AB24	MWE	
238	AA24	MRAS	
239	Y24	MDQ[5]	Pull down to VSS through high resistance.
240	W24	MDQ[1]	
241	V24	MDQ[7]	
242	U24	MDQ[10]	
243	T24	MDQ[9]	

Pin No.	JEDEC	Pin name	Process
244	R24	MDM[1]	Pull down to VSS through high resistance.
247	M24	MDQ[18]	
248	L24	MDQ[17]	
249	K24	MDQ[23]	
250	J24	MDQ[26]	
251	H24	MDQ[28]	
252	G24	MDM[3]	
253	F24	MEM_ED[1]	Pull up to VDDE or pull down to VSS through high resistance.
254	E24	MEM_ED[5]	
255	D24	MEM_ED[9]	
256	C24	MEM_ED[13]	
257	C23	MEM_EA[2]	
258	C22	MEM_EA[6]	
259	C21	MEM_EA[10]	
260	C20	MEM_EA[14]	
261	C19	MEM_EA[18]	
262	C18	MEM_EA[22]	
263	C17	MEM_XWR[0]	
264	C16	MEM_XCS[2]	
267	C13	TCK	
269	C11	TRACEDATA[1], UART_SIN5, PWM_O1	
270	C10	TRACECLK, UART_SIN3	
271	C9	DOUTB0[2]	Keep the pin open.
272	C8	DOUTB0[6]	
273	C7	DOUTG0[4]	
274	C6	DOUTR0[2]	
275	C5	DOUTR0[5]	
276	C4	DOUTR0[7]	
277	D4	DOUTB1[3], MEM_XWR[3], DOUTB0[1]	Pull up to VDDE or pull down to VSS through high resistance.
278	E4	DOUTB1[7], MEM_ED[19], DOUTR0[1]	
279	F4	DOUTG1[5], MEM_ED[23], GPIO_PD[9]	
280	G4	DOUTR1[3], MEM_ED[27], I2S_SDO0	
281	H4	DOUTR1[6], MEM_ED[30], I2S_SCK0	
282	J4	HSYNC1, DREQ[6]	
283	K4	DE1, XDACK[7]	Keep the pin open.
284	L4	VIN0[4]	Pull up to VDDE or pull down to VSS through high resistance.
285	M4	VIN0[0]	
287	P4	USB_AVSB	Connect to VSS.
288	R4	USB_AVSF2	
289	T4	USB_AVSF2	
292	W4	VIN1[3], RI1[3], CAN_TX1	Keep the pin open.

Pin No.	JEDEC	Pin name	Process
293	Y4	VIN1[0], GI1[6], I2S_WS1	Keep the pin open.
294	AA4	VINHSYNC1, I2S_SDI1	Pull up to VDDE or pull down to VSS through high resistance.
295	AB4	I2S_WS2, BI1[3], SPI_SS	Keep the pin open.
296	AC4	IDE_DINTRQ, I2S_SDO1	
297	AC5	IDE_DD[15], CAN_TX0	
298	AC6	IDE_DD[11], GPIO_PD[23]	
299	AC7	IDE_DD[7], GPIO_PD[19]	
300	AC8	IDE_DD[3], GPIO_PD[15]	
301	AC9	IDE_DA[2], Reserved (output)	
302	AC10	IDE_XDIOW, Reserved (output)	
303	AC11	MPX_MODE_1[0]	Pull up to VDDE or pull down to VSS through high resistance.
305	AC13	AD_VR0	Connect to VSS.
306	AC14	AD_VR1	
308	AC16	UART_SIN2	Pull up to VDDE or pull down to VSS through high resistance.
309	AC17	SD_CLK	Keep the pin open.
310	AC18	SD_DAT[3]	Pull up to VDDE or pull down to VSS through high resistance.
312	AC20	INT_A[2]	
313	AC21	DDRTYPE	Pull up to VDDE through high resistance.
314	AC22	ODTCONT	Keep the pin open.
315	AC23	MA[0]	
316	AB23	MCS	
317	AA23	MCAS	
318	Y23	MDQ[3]	Pull down to VSS through high resistance.
319	W23	MDQ[4]	
320	V23	MDM[0]	
321	U23	MDQ[11]	
322	T23	MDQ[12]	
323	R23	MDQ[14]	
324	P23	OCD	Keep the pin open.
325	N23	ODT	
326	M23	MDQ[19]	Pull down to VSS through high resistance.
327	L23	MDQ[20]	
328	K23	MDM[2]	
329	J23	MDQ[27]	
330	H23	MDQ[25]	
331	G23	MDQ[30]	
332	F23	MEM_ED[2]	Pull up to VDDE or pull down to VSS through high resistance.
333	E23	MEM_ED[6]	
334	D23	MEM_ED[10]	
335	D22	MEM_EA[5]	

Pin No.	JEDEC	Pin name	Process
336	D21	MEM_EA[9]	Pull up to VDDE or pull down to VSS through high reistance.
337	D20	MEM_EA[13]	
338	D19	MEM_EA[17]	
339	D18	MEM_EA[21]	
340	D17	MEM_EA[24]	
341	D16	MEM_XCS[0]	
342	D15	MEM_RDY	
344	D13	TDI	
346	D11	TRACEDATA[2], UART_SOUT4	
347	D10	RTCK	Keep the pin open.
348	D9	DOUTB0[3]	
349	D8	DOUTB0[7]	
350	D7	DOUTG0[5]	
351	D6	DOUTR0[3]	
352	D5	DOUTR0[6]	
362	P5	USB_AVDB	Connect to VDDE.
363	R5	USB_EXT12K	Pull down to VSS through 10kΩ resistance.
364	T5	USB_AVSF2	Connect to VSS.
378	AB13	AD_VRL0	
379	AB14	AD_VRL1	
391	V22	MDQ[6]	Pull down to VSS through high resistance.
398	L22	MDQ[22]	

7.2.25. Unused pin with pin multiplex function in the duplex case

PWM, I2S1, and CAN pins may be duplicated and allocated to external pin depending on pin multiplex function's group combination. In this case, follow the procedure below.

Pin No.	JEDEC	Pin multiplex group: pin name	Process
122	AC2	Pin multiplex group #2:PWM_O1	Keep the pin open.
123	AD2	Pin multiplex group #2:PWM_O0	
220	AD9	Pin multiplex group #4:PWM_O1	
131	AE9	Pin multiplex group #4:PWM_O0	
269	C11	Pin multiplex group #5:PWM_O1	Pull down to VSS through high resistance.
184	B11	Pin multiplex group #5:PWM_O0	
118	W2	Pin multiplex group #2:CAN_TX0	Keep the pin open.
292	W4	Pin multiplex group #2:CAN_TX1	
209	W3	Pin multiplex group #2:CAN_RX0	
119	Y2	Pin multiplex group #2:CAN_RX1	
297	AC5	Pin multiplex group #4:CAN_TX0	
127	AE5	Pin multiplex group #4:CAN_TX1	
216	AD5	Pin multiplex group #4:CAN_RX0	
30	AF5	Pin multiplex group #4:CAN_RX1	
210	Y3	Pin multiplex group #2:I2S_SCK1	
293	Y4	Pin multiplex group #2:I2S_WS1	
211	AA3	Pin multiplex group #2:I2S_ECLK1	Pull down to VSS through high resistance.
294	AA4	Pin multiplex group #2:I2S_SDI1	
22	AB1	Pin multiplex group #2:I2S_SDO1	Keep the pin open.
28	AF3	Pin multiplex group #4:I2S_SDI1	Pull down to VSS through high resistance.
125	AE3	Pin multiplex group #4:I2S_WS1	Keep the pin open.
215	AD4	Pin multiplex group #4:I2S_ECLK1	Pull down to VSS through high resistance.
214	AD3	Pin multiplex group #4:I2S_SCK1	Keep the pin open.
296	AC4	Pin multiplex group #4:I2S_SDO1	

8. Electrical Characteristics

8.1. Maximum Ratings

Table 8-1, Table 8-2, and Table 8-3 show the maximum ratings.

Table 8-1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	VDDI, PLLVDD VDDE DDRVDE	-0.5 to 1.8 (*1) -0.5 to 4.0 (*2) -0.5 to 2.5 (*3)	V
Input voltage	V_I	-0.5 to VDDI + 0.5 (< 1.8V) -0.5 to VDDE + 0.5 (< 4.0V) -0.5 to DDRVDE + 0.5 (< 2.5V)	V
Output voltage	V_O	-0.5 to VDDI + 0.5 (< 1.8V) -0.5 to VDDE + 0.5 (< 4.0V) -0.5 to DDRVDE + 0.5 (< 2.5V)	V
Storage temperature	T_{ST}	-55 to 125	°C
Junction temperature	T_J	-40 to 125	°C
Power consumption	P_D	1.5	W
Supply current	I_D	1.2V: 690.1 (*4) 1.8V: 508 (*4) 3.3V: 125.3 (*4)	mA

*1: Power supply for internal part or PLL
*2: Power supply for I/O part
*3: Power supply for SSTL_18 I/O part
*4: Current specification necessary for each voltage power supply

Note:

- Applying stress exceeding the maximum ratings (voltage, current, temperature, etc.) may cause damage to semiconductor devices. Never exceed the ratings above.
- Since thermal destruction of elements might occur, do not connect IC output or I/O pin directly, or connect them to V_{DD} or V_{SS} directly, except the pin designed output timing to prevent such incident.
- Provide ESD protection, such as grounding when handling the product; otherwise externally-charged electric charge flows into the IC and discharges, which may cause circuit destruction.
- Applying voltage higher than V_{DD} or lower than V_{SS} to I/O pins of CMOS IC, or applying voltage higher than the ratings between V_{DD} and V_{SS} may cause latch up. The latch up increases supply current, resulting in thermal destruction of elements. When handling the product, never exceed the maximum ratings.

Table 8-2 ADC Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	AD_AVD0	-0.5 to 4.0	V
Input voltage	AD_VRH0 AD_VRH1 AD_VRL0 AD_VRL1 AD_VIN0 AD_VIN1	-0.5 to VDDE + 0.5 (< 4.0V)	V
Output voltage	AD_VR0 AD_VR1	-0.5 to VDDE + 0.5 (< 4.0V)	V
Junction temperature	T_J	-40 to 125	°C

The maximum ratings of USB PHY are shown in Table 8-3.

Table 8-3 USB2.0 Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	USB_AVDF1 USB_AVDB	V_{SS}--0.5 to 4.0	V
	USB_AVDF2 USB_AVDP	V_{SS}--0.5 to 1.8	V
Junction temperature	T_J	-40 to 125	°C
Supply current	USB_AVDF1 USB_AVDB	Total 37.5	mA
	USB_AVDF2	19.2	mA
	USB_AVDP	13.0	mA

The maximum ratings are the limits that must not be exceeded. As long as USB PHY is used within the range predetermined in the maximum ratings, it never suffers permanent damage. However, this does not assure normal logic operation.

8.2. Recommended Operating Conditions

Table 8-4 3.3V Standard CMOS I/O Recommended Operating Conditions

Parameter		Symbol	Rating			Unit
			Min.	Typ.	Max.	
Power supply voltage		VDDE VDDI, PLLVDD	3.0 1.1	3.3 1.2	3.6 1.3	V
Input voltage (High level)	3.3V CMOS	VIH	2.0	–	VDDE + 0.3	V
Input voltage (Low level)	3.3V CMOS	VIL	-0.3	–	0.8	V
Operating ambient temperature		T_A	-40	–	85	°C
Junction temperature		T_J	-40	–	125	°C

Table 8-5 SSTL_18 Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VDE (DDRVDE)	1.7	1.8	1.9	V
	VDDI	1.10	1.20	1.30	V
Junction temperature	T_J	-40	–	125	°C

The recommended operating conditions for the standard SSTL_18 (excerpted from JESD8-15a).

Table 8-6 USB2.0 Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply voltage	USB_AVDF1 USB_AVDB	3.0	3.3	3.6	V
	USB_AVDF2	1.1	1.2	1.3	V
	USB_AVDP	1.1	1.2	1.3	V
Junction temperature	T_J	-40	–	125	°C

Clock to be input to USB_CRYCLK48 should meet followings:

- 48MHz±100ppm clock
- 100ps or less jitter

Note:

The recommended operating conditions are primarily intended to assure the normal operation of semiconductor device. The values of electrical characteristics are guaranteed under the requirements above, so use the product accordingly. Using the product without observing the conditions may affect the product's reliability.

Performance of this product is not guaranteed using under the unspecified conditions and unspecified combination of logic. Be sure to contact Fujitsu when using the product under such conditions.

8.3. Precautions at Power On

8.3.1. Recommended Power On/Off Sequence

Follow the power on/off sequence as shown below:

<ON>: VDDI (internal and PLLVDD) → DDRVDE (external) → VDDE (external) → Signal

<OFF>: Signal → VDDE (external) → DDRVDE (external) → VDDI (internal and PLLVDD)

Figure 8-1 Recommended Power On/Off Sequence (1)

There is no limitation on the sequence of power on/off of VDDI, VDDE, and DDRVDE if the following condition is met. (Figure 8-2)

- Do not apply VDDE and DDRVDE (external) continuously more than 1 second when VDDI (internal) is off.

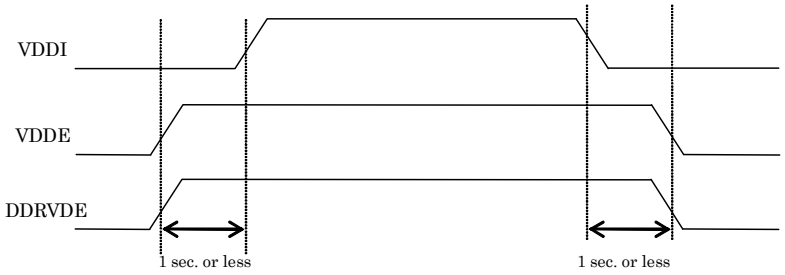


Figure 8-2 Recommended Power On/Off Sequence (2)

Perform power on/off for VREF according to the DDR2-SDRAM regulation.
Perform power on/off so that power for PLLVDD (PLL) does not exceed VDDI.
Turn on all power. Turning on only a part of them is prohibited.
CMOS IC becomes unstable immediately after power-on so that proceed reset immediately.
Set the reset pins (XTRST and XRST) to Low when power-on.
Input clock to CLK pin immediately after power-on.
It requires at least 100 clocks (input clock to CLK pin) for the reset signal "L" applied to the XRST pin to be transmitted to all internal circuits.

8.3.2. Power On Reset

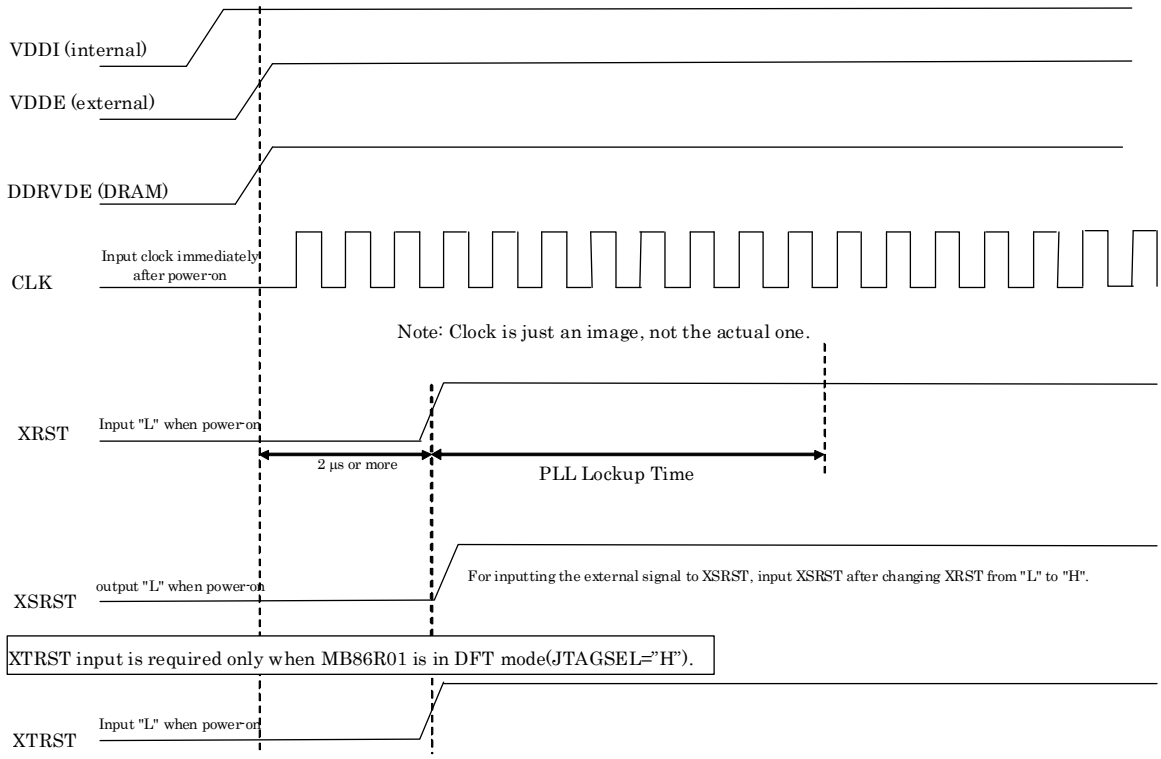


Figure 8-3 Power On Sequence

Input XRST pin to Low when power-on.
Keep XRST pin High after setting to Low level for 2µs or more.
Access the other registers or memory controller after PLL Lockup Time.

When MB86R01 is in DFT mode, XTRST should be input as well as XRST.

8.4. DC Characteristics

8.4.1. 3.3V Standard CMOS I/O

Table 8-7 shows 3.3V standard CMOS I/O DC characteristics.

Table 8-7 Standard CMOS I/O DC Characteristics

Measurement condition: VDDE = 3.3 ±0.3V, VSS = 0V, T_J = -40 to 125°C

Parameter	Symbol	Condition		Rating			Unit
				Min.	Typ.	Max.	
H level input voltage	VIH			2.0	–	VDDE + 0.3	V
L level input voltage	VIL			-0.3	–	0.8	V
H level output voltage	VOH	IOH = -100µA		VDDE - 0.2	–	VDDE	V
L level output voltage	VOL	IOL = 100µA		0	–	0.2	V
H level output V-I characteristic	–	Driving capability 1	IOH = 4mA	See Figure 8-4, Figure 8-5, and Figure 8-6 characteristics			–
		Driving capability 2	IOH = 6mA				
		Driving capability 3	IOH = 8mA				
L level output V-I characteristic	–	Driving capability 1	IOL = 4mA				–
		Driving capability 2	IOL = 6mA				
		Driving capability 3	IOL = 8mA				
Input leakage current	IL			–	–	±4	µA

Driving capabilities 1 to 3 in the table above indicate the following external pins:

Driving capability 1: TDO, MEM_EA[24:1], MEM_ED[15:0], MEM_RDY, MEM_XCS0, MEM_XCS2, MEM_XCS4, MEM_XRD, MEM_XWR0, MEM_XWR1

Driving capability 2: VINHSYNC0, VINVSYNC0, I2S_ECLK2, I2S_SCK2, I2S_SDO2,I2S_WS2, IDE_DD[15:0], IDE_DINTRQ, IDE_XCBLID, IDE_XDASP, PWM_O0, PWM_O1, VIN10-7, VINFID1, DOUTB1[7:2], DOUTG1[7:2], DOUTR1[7:2], GV1, HSYNC0, HSYNC1, SD_CMD, SD_DAT[3:0], TRACECLK, TRACEDATA[3:0], VIN0[7:0], VSYNC0, VSYNC1, XSRST, DE0, DE1, DOUTB0[7:2], DOUTG0[7:2], DOUTR0[7:2], GV0, IDE_CSEL, IDE_DA[2:0], IDE_XDCS[1:0], IDE_XDDMACK, IDE_XDIOR, IDE_XDIOW, IDE_XDRESET, RTCK, SD_CLK, TRACECTL, UART_SOUT[2:0], UART_XRTS0, USB_PRTPWR

Driving capability 3: DCLKO[1:0]

8.4.1.1. 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 1)

Conditions	MIN:	Process = Slow	T_J = 125°C	VDDE = 3.0 V
	TYP:	Process = Typical	T_J = 25°C	VDDE = 3.3 V
	MAX:	Process = Fast	T_J = -40°C	VDDE = 3.6 V

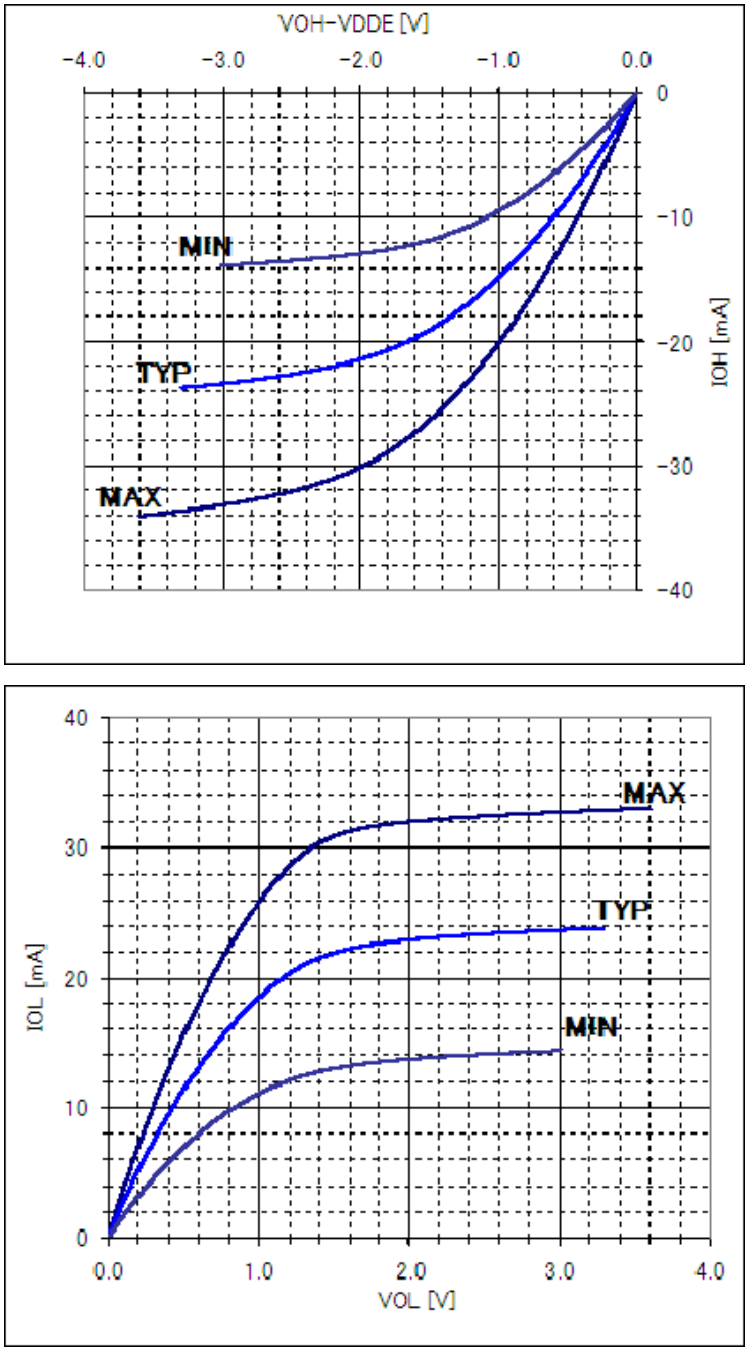


Figure 8-4 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 1)

8.4.1.2. 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 2)

Conditions	MIN:	Process = Slow	T_J = 125°C	VDDE = 3.0 V
	TYP:	Process = Typical	T_J = 25°C	VDDE = 3.3 V
	MAX:	Process = Fast	T_J = -40°C	VDDE = 3.6 V

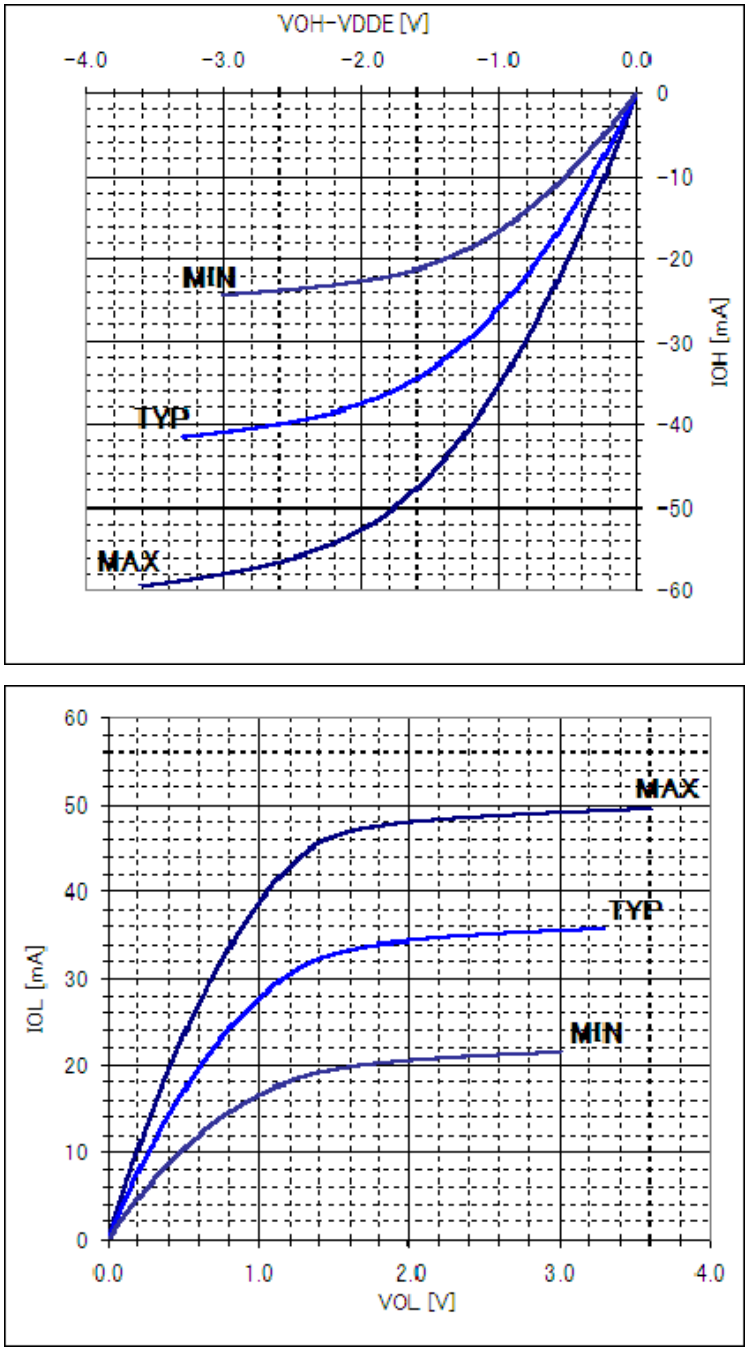


Figure 8-5 3.3V Standard CMOS I/O V-I Characteristic (Driving Capability 2)

8.4.1.3. 3.3V Standard CMOS I/O V-I Characteristics (Driving Capability 3)

Conditions	MIN:	Process = Slow	T_J = 125°C	VDDE = 3.0 V
	TYP:	Process = Typical	T_J = 25°C	VDDE = 3.3 V
	MAX:	Process = Fast	T_J = -40°C	VDDE = 3.6 V

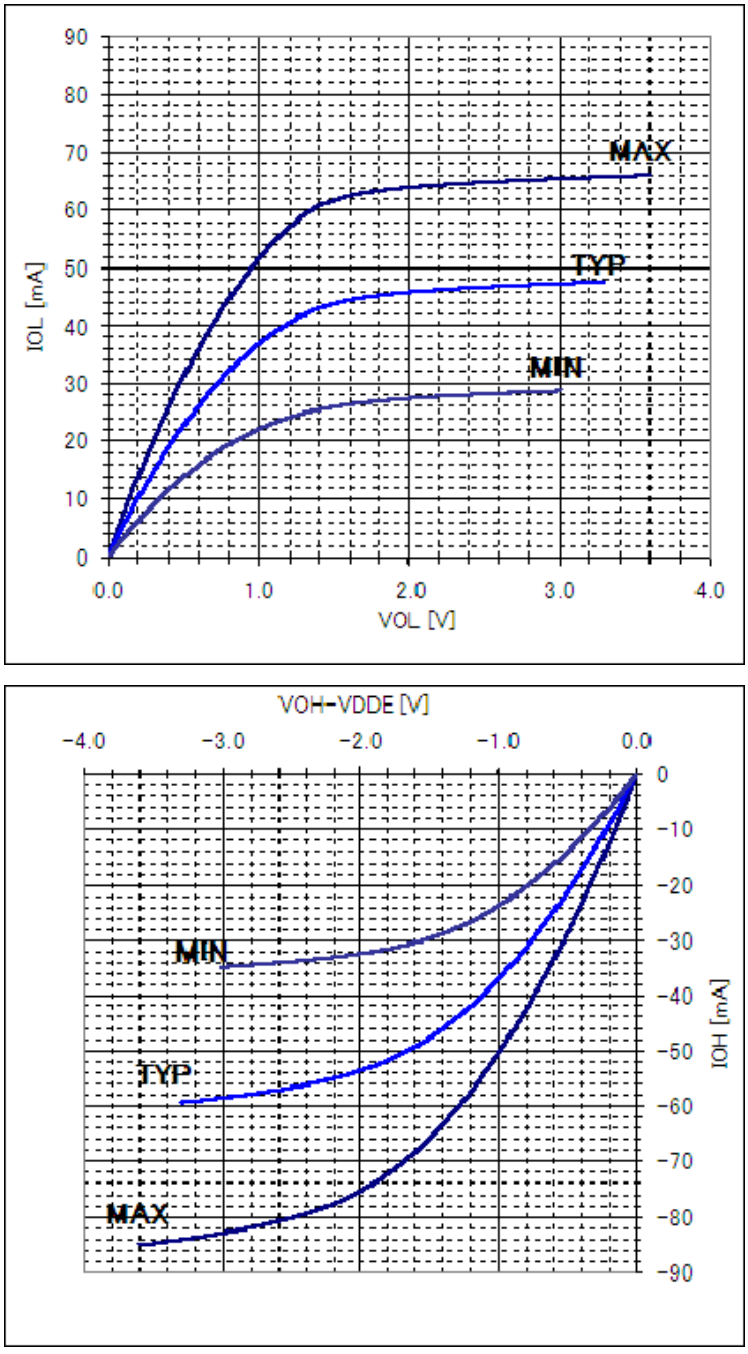


Figure 8-6 3.3 V Standard CMOS I/O V-I Characteristic (Driving Capability 3)

8.4.2. DDR2SDRAM IF I/O (SSTL_18)

SSTL_18 DC characteristics (excerpted from JESD8-15a).

Table 8-8 SSTL18 Input DC Logic Levels (Single Ended)

Symbol	Parameter	Min.	Max.	Unit
VIH (DC)	DC input logic High	VREF + 125	VDDQ + 300	mV
VIL (DC)	DC input logic Low	-300	VREF - 125	mV

Table 8-9 SSTL18 Input AC Logic Levels (Single Ended)

Symbol	Parameter	Min.	Max.	Unit
VIH (AC)	AC input logic High	VREF + 250	–	mV
VIL (AC)	AC input logic Low	–	VREF - 250	mV

Table 8-10 SSTL18 Input AC Test Conditions (Single Ended)

Symbol	Condition	Value	Unit
VREF	Input reference voltage	0.5 × VDDQ	V
VSWING (max.)	Input single maximum peak to peak swing	1.0	V
SLEW	Input single minimum slew rate	1.0	V/ns

Table 8-11 SSTL18 Input DC Logic Levels (Differential Ended)

Symbol	Parameter	Min.	Max.	Unit
VIN (DC)	DC input signal voltage	-300	VDDQ + 300	mV
VID (DC)	DC differential input voltage	250	VDDQ + 600	mV

Table 8-12 SSTL18 Input AC Logic Levels (Differential Ended)

Symbol	Parameter	Min.	Max.	Unit
VID (AC)	AC differential input voltage	500	VDDQ + 600	mV
VIX (AC)	AC differential cross point voltage	0.5 × VDDQ - 175	0.5 × VDDQ + 175	mV

Table 8-13 SSTL18 Input AC Test Conditions (Differential Ended)

Symbol	Parameter	Min.	Max.	Unit
Vr	Input timing measurement reference level	VIX (cross point)		V
VSWING	Input signal peak to peak swing voltage	–	1.0	V
SLEW	Input signal slew rate	1.0	–	V/ns

Table 8-14 SSTL18 Output DC Current Drive

Symbol	Parameter	Min.	Max.	Unit	Notes
IOH (DC)	Output minimum source DC current	-11.4 (*3)	–	mA	(*1)
IOL (DC)	Output minimum sink DC current	11.4 (*3)	–	mA	(*2)

*1: VDDQ = 1.7V, VOUT = 1420mV
*2: VDDQ = 1.7V, VOUT = 280mV
*3: The value is different from JESD8-15a. (JESD8-15a: ±13.4mA)

Table 8-15 SSTL18 Differential AC parameters

Symbol	Parameter	Min.	Max.	Unit
VOX	AC differential cross point voltage	0.5 × VDDQ - 125	0.5 × VDDQ + 125	mV

Note:

External pin for DDR2SDRAM IO buffer is as follows.

MDQSP[3:0], MDQSN[3:0], MDM[3:0], MDQ[31:0], MCKP, MCKN, MA[13:0], MBA[1:0], MCAS, MCKE, MCS, MRAS, MWE, ODTCONT, OCD, ODT, VREF0, VREF1

8.4.3. ADC

Table 8-16 Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	AD_AVD0	2.70	3.00	3.60	V
Reference voltage (H)	AD_VRH0 AD_VRH1	AD_AVD0*0.75	–	AD_AVD0	V
Reference voltage (L)	AD_VRL0 AD_VRL1	V_{SS} (*1)	–	AD_AVD0*0.25	V
Decoupling capacitor	AD_VR0 (*2) AD_VR1 (*2)	0.05	–	–	µF
Analog input voltage	AD_VIN0 AD_VIN1	AD_VRL0 AD_VRL1	–	AD_VRH0 AD_VRH1	V
Analog input frequency	AD_VIN0 AD_VIN1	0	–	500	kHz

Note:

*1: V_{SS} = AD_AVS1 (analogue GND)

*2: In the case that VR is decoupled with AVS by decoupling capacitor, A/D outputs incorrect result at immediately after power-on or at the resumption from power down mode.
Because charge current for decoupling capacitors is supplied through the reference resistance, it takes about 2ms to get correct result (it is the case decoupling capacitor is 0.1µF.).

Table 8-17 ADC Characteristics

(VDD = 1.2V, AVD = 3.0V, FS = 100KS/s, FC = 1.4MHz, FVIN = 1 kHz, T_A = 25°C (*1))

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Supply current (included reference current)	AD_AVD0	–	0.8	1.2	mA
		-1	–	50	µA
Reference voltage (M)	AD_VR0 AD_VR1	–	AD_AVD0/2	–	V
		-3	–	3	%
Reference resistance	AD_VRH0 AD_VRH1 AD_VRL0 AD_VRL1	7.3	9	10.7	kΩ
Zero transition voltage (*2)		Typ. -20	AD_VRL0+1LSB AD_VRL1+1LSB	Typ. +20	mV
Full scale transition Voltage (*2)		Typ. -20	AD_VRH0-1LSB AD_VRH1-1LSB	Typ. +20	mV
Integral non linearity (*3)		-2.0	–	+2.0	LSB
Differential non linearity (*3)		-1.5	–	+1.5	LSB

*1: VR is connected to AVS with decoupling capacitor (0.1µF).
Unique voltage is supplied to VRH and VRL by voltage source.

*2: VZT and VFST are dependent on chip layout and wiring resistance.

*3: 1LSB = (VFST-VZT)/1022, INLn = ((1LSBxn + VZT) - Vn)/1LSB, DNLn = (Vn + 1 -Vn)/1LSB - 1

8.4.4. I^2C Bus Fast Mode I/O

Table 8-18 I^2C I/O DC Characteristics

Parameter & Condition	Symbol	Standard Mode		Fast Mode (*1)		Unit
		Min.	Max.	Min.	Max.	
"L" level input voltage	VIL	-0.5	0.3 VDDE	-0.5	0.3 VDDE	V
"H" level input voltage	VIH	0.7 VDDE	(*2)	0.7 VDDE	(*2)	V
Schmitt trigger hysteresis VDDE > 2[v]	Vhys	n/a	n/a	0.05 VDDE	–	V
"L" level output voltage Sink current 3[mA] VDDE > 2[v]	VOL1	0	0.4	0	0.4	V
Output slew rate (Tfall) Bus capacitance 10[pF] ~ 400[pF] VIH (min.) to VIL (max.)	tof	–	250	20 + 0.1Cb (*3)	250	ns
Data line leakage Input voltage 0.1 ~ 0.9 VDDE (max.)	Ii	-10	10	-10	10	µA
I/O pin capacitance	Ci	–	10	–	10	pF

*1: The I^2C Bus Fast Mode I/O buffer is downward compatible with standard mode.
*2: 90nm Technology: Complies with the maximum ratings 4[V].
*3: Cb: Capacitance for 1 bus line (Unit: pF).
*4: The I^2C Bus Fast Mode I/O buffer itself has no function to prevent spike of 50ns pulse width (max.). Therefore, provide any input filter to prevent spike for both internal and external semiconductor device.

Note:

External pin for I^2C IO buffer is as follows.

I2C_SCL0, I2C_SDA0, I2C_SCL1, I2C_SDA1

8.4.4.1. I^2C IO V-1 Characteristic Figure

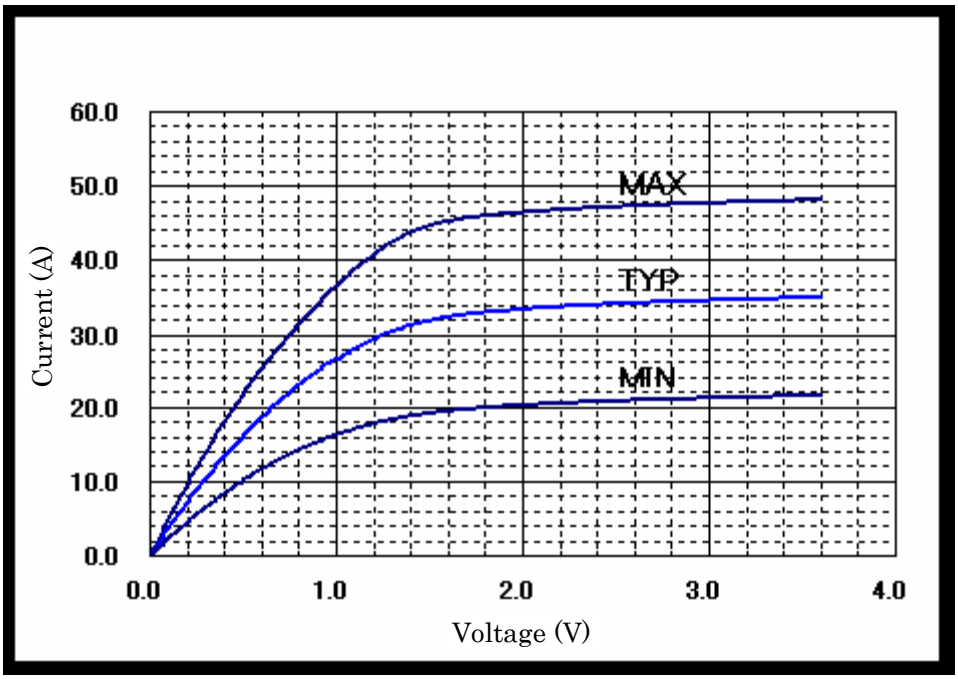


Figure 8-7 I^2C V-I Characteristic Figure

8.4.5. USB2.0

Table 8-19 Recommended Operating Conditions (High-speed)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input levels for high-speed:					
high-speed squelch detection threshold (differential signal amplitude)	VHSSQ	100	–	200	mV
High-speed disconnect detection threshold (differential signal amplitude)	VHSDSC	525	–	625	mV
High-speed differential input signaling levels (this spec is based on "Template 6")		150 (the absolute value)	–	–	mV
High-speed data signaling common mode voltage range (guideline for receiver)	VHSCM	-50	–	500	mV
Output levels for high-speed:					
High-speed idle level	VHSOI	-10.0	–	10.0	mV
High-speed data signaling high	VHSOH	360	–	440	mV
High-speed data signaling low	VHSOL	-10.0	–	10.0	mV
Chirp J level (differential voltage)	VCHIRPJ	700	–	1100	mV
Chirp K level (differential voltage)	VCHIRPK	-900	–	-500	mV
Terminations in high-speed:					
Termination voltage in high-speed	VHSTERM	-10	–	10	mV

Table 8-20 Recommended Operating Conditions (Full-speed/Low-speed)

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Input levels for full-speed/low-speed:					
High (driving)	VIH	2.0	–	–	V
High (floating)	VIHZ	2.7	–	3.6	V
Low	VIL	–	–	0.8	V
Differential input sensitivity	VDI	0.2	–	–	V
Differential common mode range	VCM	0.8	–	2.5	V
Output levels for full-speed/low-speed:					
Low	VOL	0.0	–	0.3	V
High (driven)	VOH	2.8	–	3.6	V
SE1	VOSE1	0.8	–	–	V
Output signal crossover voltage	VCRS	1.3	–	2.0	V
Input capacitance for full-speed/low-speed:					
Downstream facing port (being shared with upstream facing port at device mode, so the less value is selected as the maximum spec)	CIND (CINUB)	–	–	100	pF
Transceiver edge rate control capacitance	CEDGE	–	–	75	pF
Terminations in full-speed/low-speed:					
Bus pull-up resistor on upstream port (idle bus) (this is used only in the device mode (HOSTMODE = "0" setting).)	RPUI	0.9	–	1.575	kΩ
Bus pull-up resistor on upstream port (upstream port receiving) (this is used only in the device mode (HOSTMODE = "0" setting).)	RPUA	1.425	–	3.090	kΩ
Input impedance exclusive of pull-up/pull-down	ZINP	300	–	–	kΩ
Termination voltage on upstream port pull-up	VTERM	3.0	–	3.6	V

8.5. AC CHARACTERISTIC

In this chapter, the AC timing of external ports is described.

8.5.1. Memory Controller Signal Timing

Table 8-21 Memory Controller AC Timing

Signal Name	Symbol	Description	Value			Unit
			Min	Typ	Max	
MEM_XCS0 MEM_XCS2 MEM_XCS4	t_{cso}	Chip Select delay time	–	–	10	ns
MEM_EA[24:1]	t_{ao}	Address delay time	–	–	11	ns
MEM_ED[31:0]	t_{do}	Data output delay time	–	–	11	ns
	t_{doz}	Data output HiZ time	–	–	12	ns
	t_{dsr}	SRAM/NOR Flash data setup time	12	–	–	ns
	t_{dhr}	SRAM/NOR Flash data hold time	0	–	–	ns
	t_{dsp}	NOR Flash page Read data setup time	13	–	–	ns
	t_{dhp}	NOR Flash page Read data hold time	0	–	–	ns
MEM_XRD	t_{rdo}	XRD delay time	–	–	10	ns
MEM_XWR[3:0]	t_{wro}	XWR delay time	–	–	10	ns

Standard clock of output delay is internal clock.
Standard clock of MEM_RDY is internal clock.

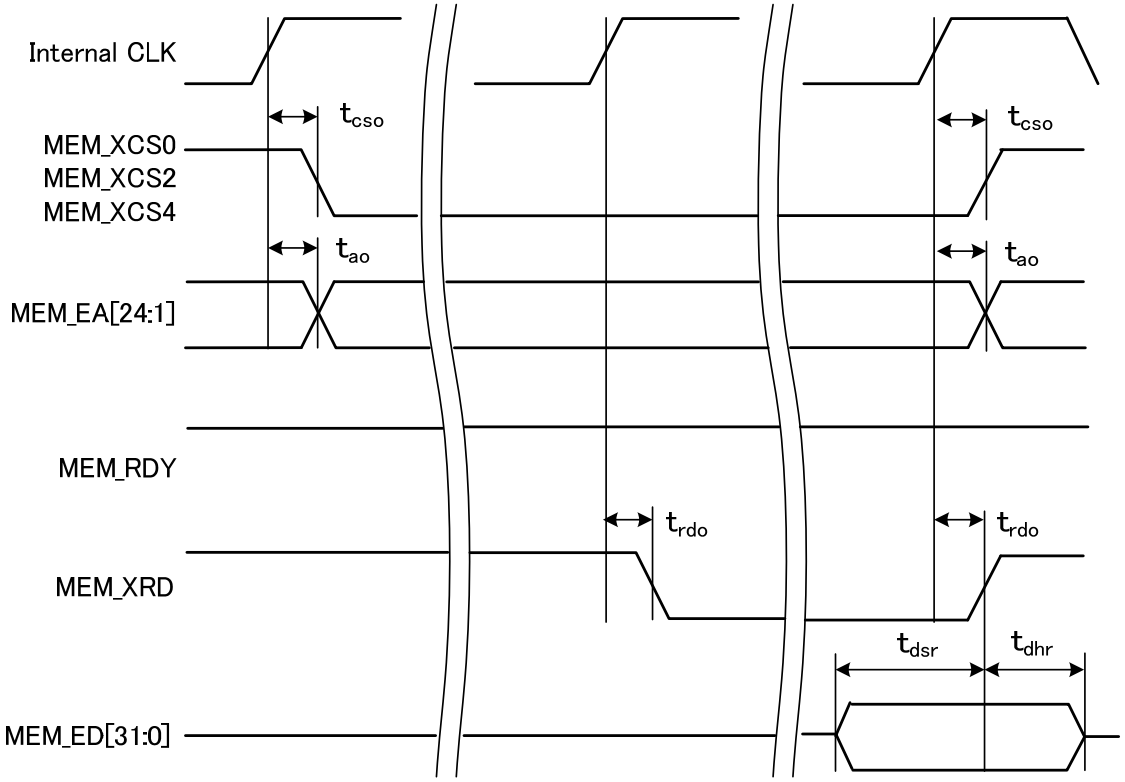


Figure 8-8 SRAM/NOR Flash Read

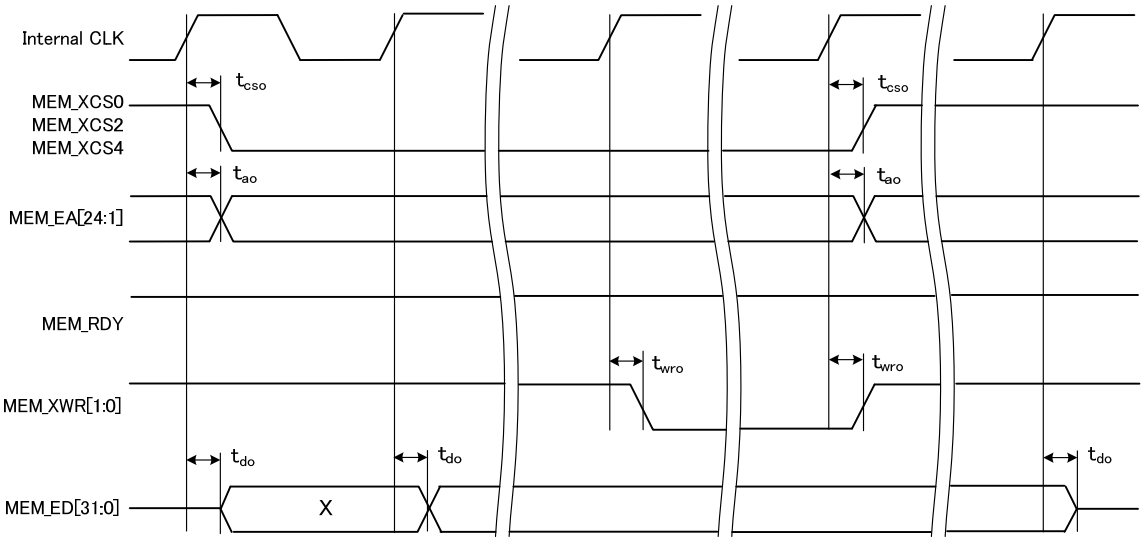


Figure 8-9 SRAM/NOR Flash Write

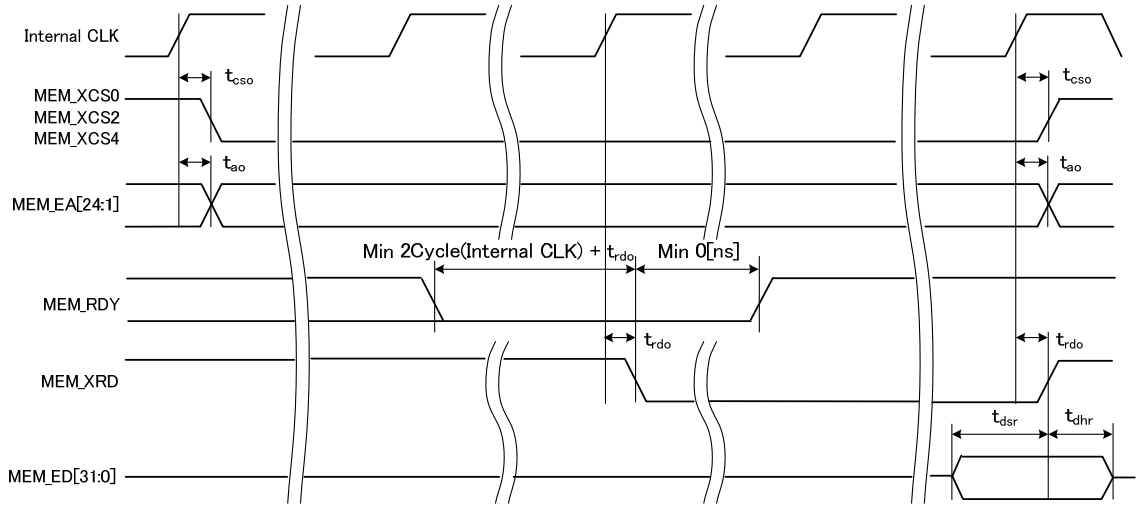


Figure 8-10 Low speed device Read

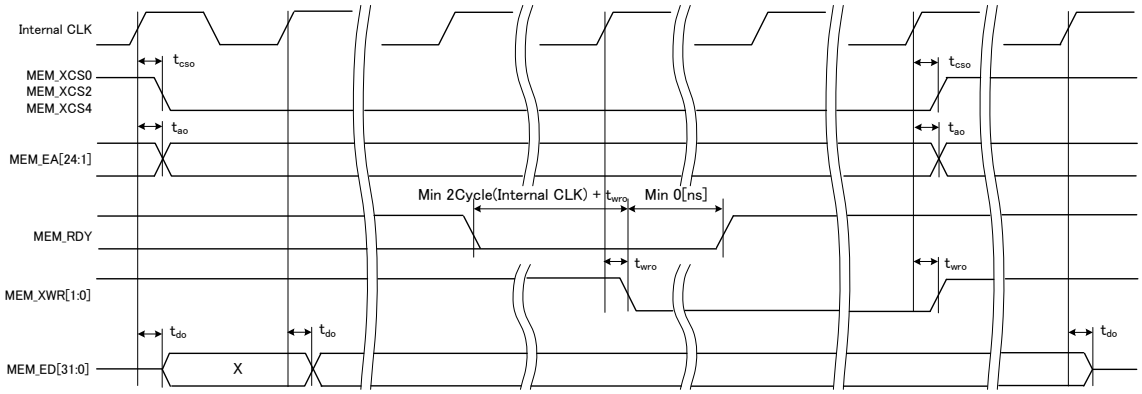


Figure 8-11 Low speed device Write

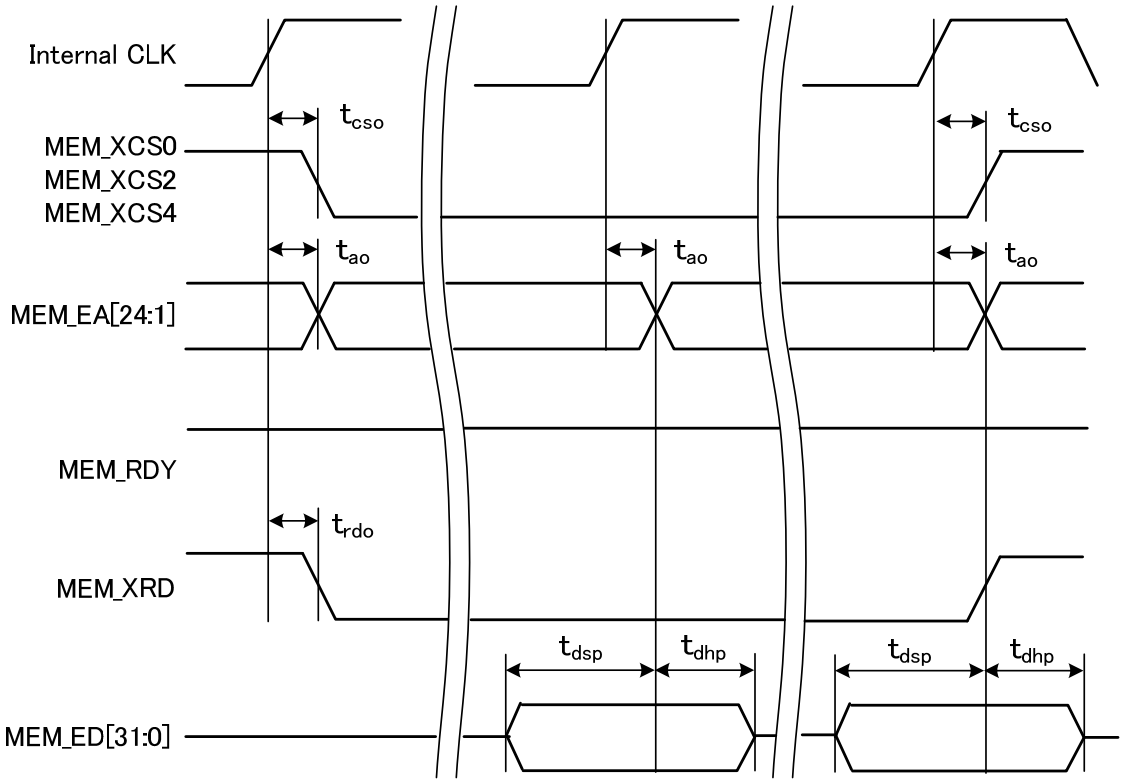


Figure 8-12 NOR Flash Page Read

8.5.2. DDR2SDRAM IF

This is able to connect with DDR2 SDRAM which is in conformance with DDR2-400 in the JEDEC (JESD79-2C.) Timing regulation is described below, and output load condition is according to the PCB design guideline.

Table 8-22 Write Spec (1 and 2): CK-CMD/ADD and CK-DQS

Item	Symbol	Spec formula	Criteria value (*1)			Unit
			Min.	Typ.	Max.	
CMD/ADD setup valid-data from CK↑	tVD_setup_CMD	(tCK/2) - 828	2172	–	–	ps
CMD/ADD hold valid-data from CK↑	tVD_hold_CMD	(tCK/2) - 545	2455	–	–	ps
Skew between DQS↑ vs. CK↑	tSkew_DQS_CK	Not tCK dependent	-1083	–	772	Ps

*1: Spec for tck = 6ns (333Mbps) is indicated

Table 8-23 Write Spec (3): DQ-DQS

Item	Symbol	Spec formula	Criteria value (*1)			Unit
			Min.	Typ.	Max.	
DQ/DM setup valid-data from DQS	tVD_setup_DQ	(tCK/4) - 884	616	–	–	ps
DQ/DM hold valid-data from DQS	tVD_hold_DQ	(tCK/4) - 776	724	–	–	ps

*1: Spec for tck = 6ns (333Mbps) is indicated

Table 8-24 Read Spec (1): DQ-DQS

Item	Symbol	Spec formula	Criteria value (*1)			Unit
			Min.	Typ.	Max.	
tSETUP DQ from DQS	tSETUP_DQ	- (0.1875*tCK – 208)	-917	–	–	ps
tHOLD DQ from DQS	tHOLD_DQ	0.1875*tCK + 503	1628	–	–	Ps

*1: Spec for tck = 6ns (333Mbps) is indicated

Table 8-25 Read Spec (2): DQ-R.T.T (RoundTrip Time)

Item	Symbol	Spec formula	Criteria value (*1)			Unit
			Min.	Typ.	Max.	
DQS RoundTripTime @CL = 3 (CK_out DRAM DQS_in)	tRTT_DQS	<Max.> 1112 <Min.> -595	-355	–	+1426	ps

*1: Spec for tck = 6ns (333Mpbs) is indicated
*2: Spec shows total delay value including tDQSCK delay of DRAM

8.5.2.1. DDR2SDRAM IF Timing Diagram

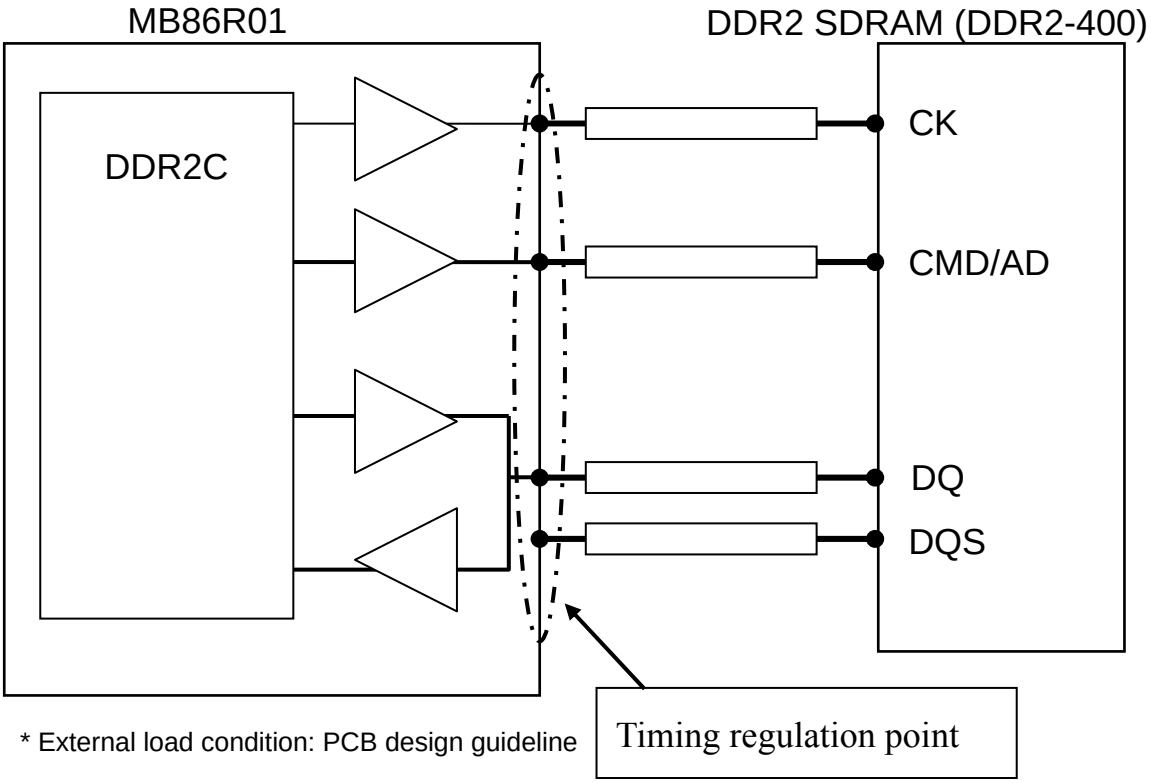


Figure 8-13 Timing Regulation Point

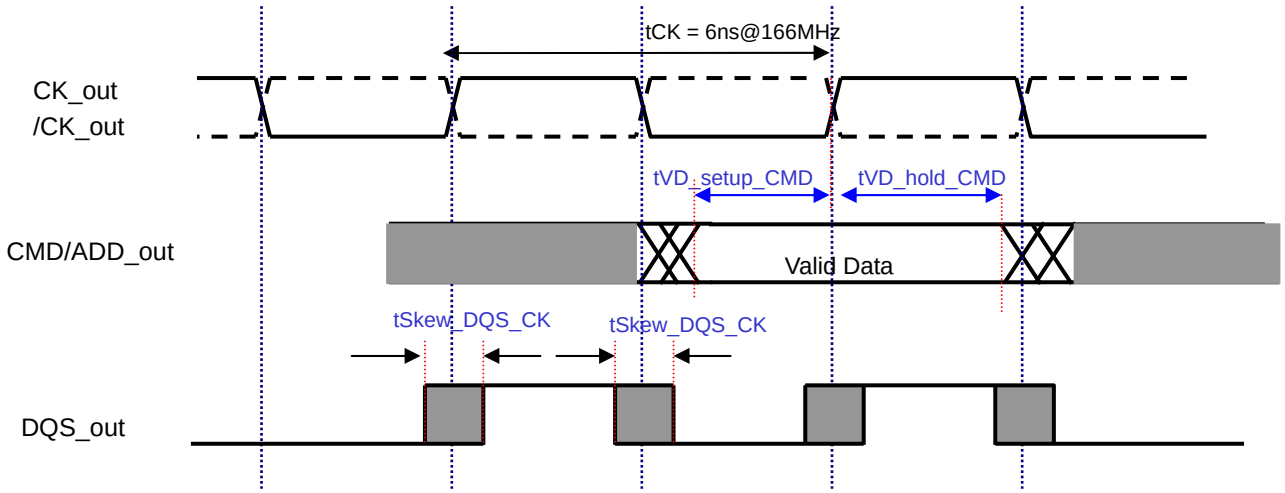


Figure 8-14 Write Spec (1 and 2): CK-CMD/ADD and CK-DQS

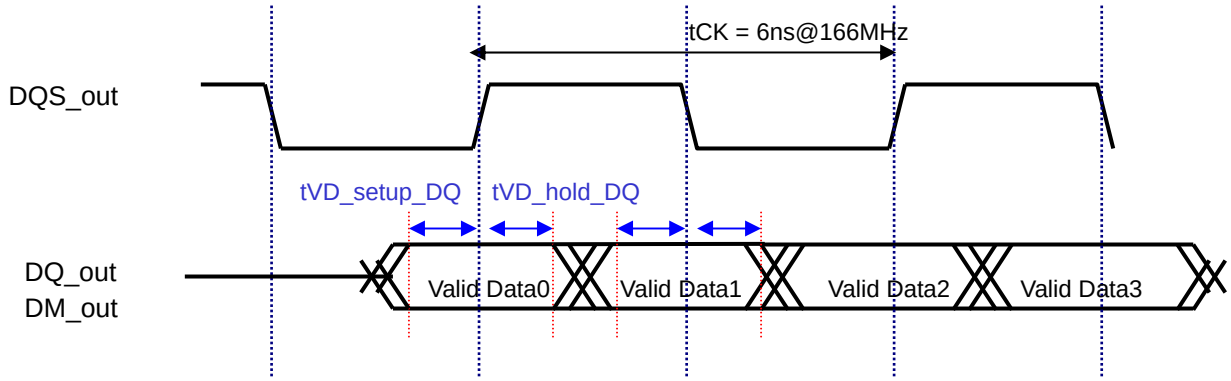


Figure 8-15 Write Spec (3): DQ-DQS

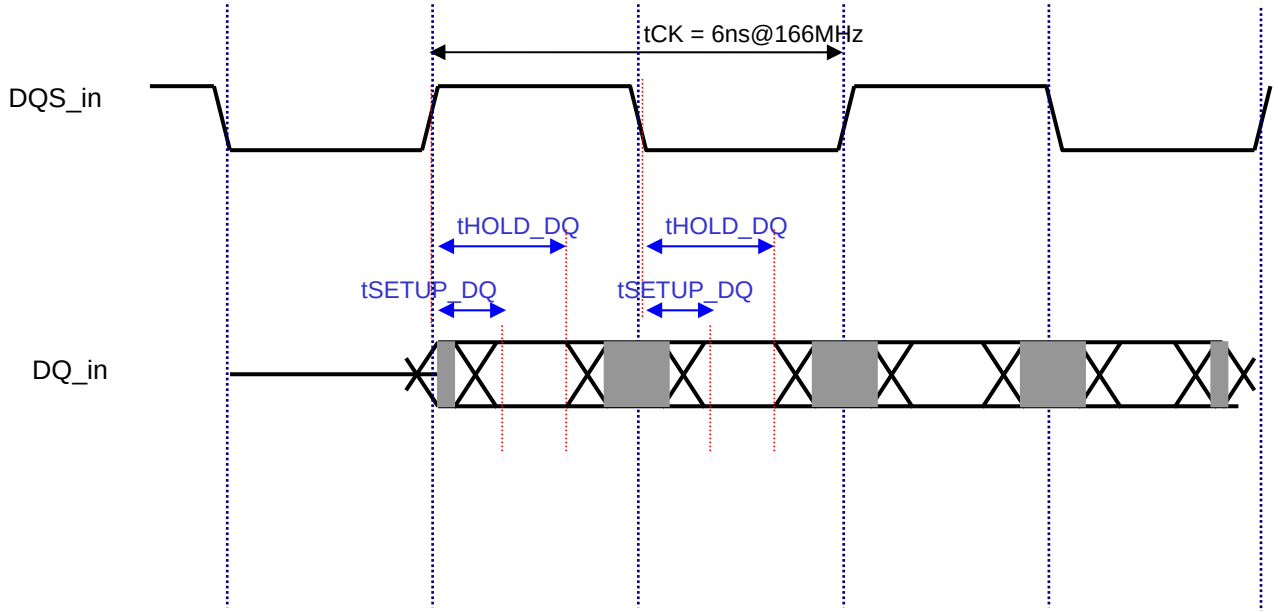


Figure 8-16 Read Spec (1): DQ-DQS

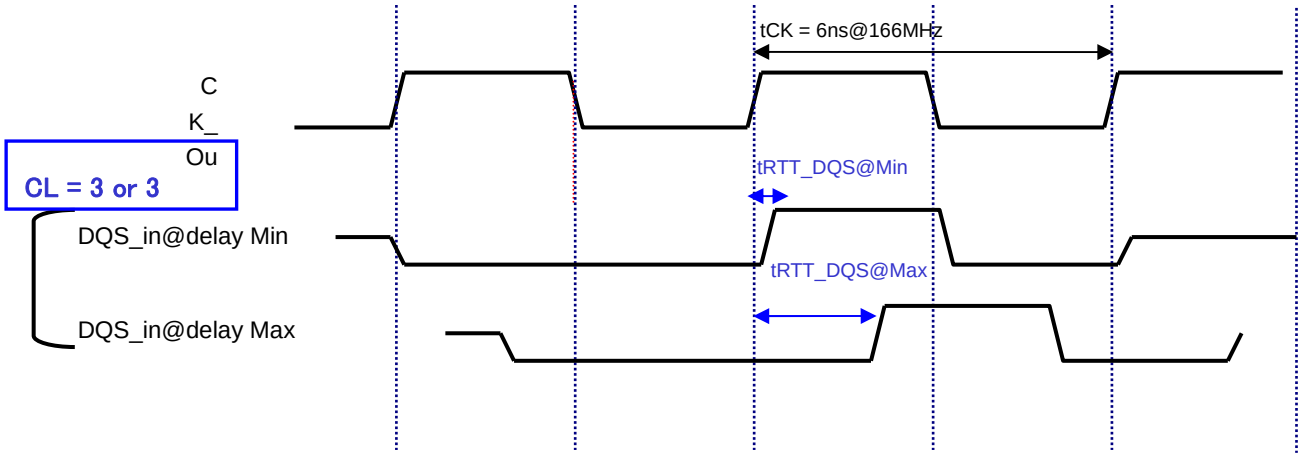


Figure 8-17 Read Spec (2): DQS-R.T.T (RoundTrip Time)

8.5.3. GPIO Signal Timing

Table 8-26 AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
GPIO_PD[23:0]	t_{do}	Data output delay time	–	–	13	ns
	t_{dw}	Input data-width	A	–	–	Ns

Internal clock is the standard of output delay.
A indicates APB bus clock cycle, and it is different from the output delay standard clock.

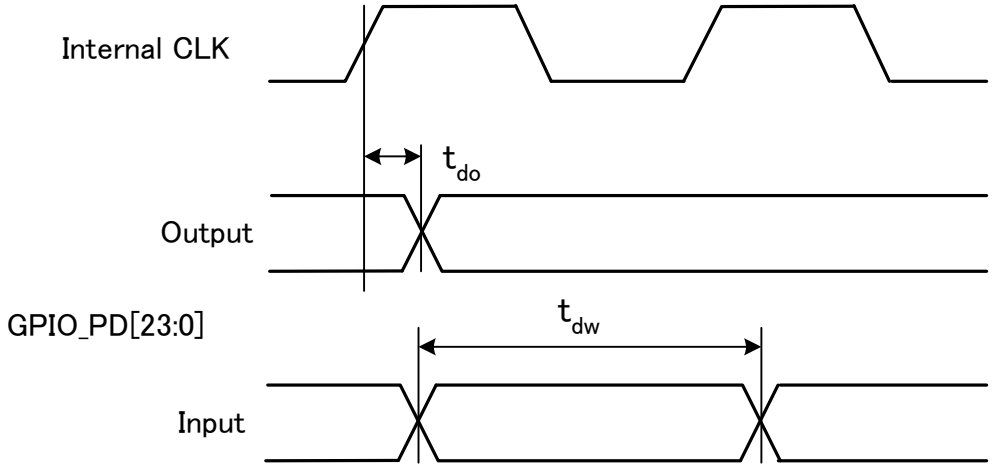


Figure 8-18 GPIO Timings

8.5.4. PWM Signal Timing

8.5.4.1. Output Signal

Table 8-27 AC Timing of Ide Data Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
PWM_O0	T0	Output delay of PWM_O0 based on APB-BusClock	2.0	–	14.0	ns
PWM_O1	T1	Output delay of PWM_O1 based on APB-BusClock	2.0	–	14.0	ns

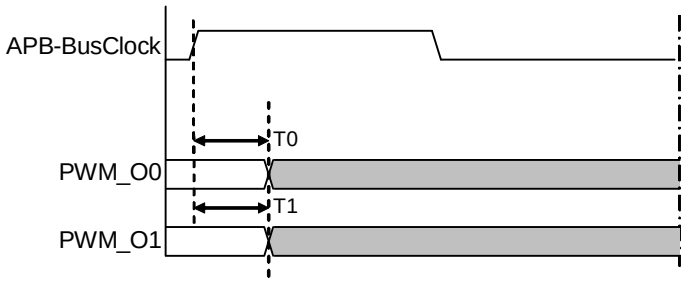


Figure 8-19 PWM Output Timing

8.5.5. GDC Display Signal Timing

8.5.5.1. Clock

Table 8-28 AC timing of Video Interface Clock Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
DCLKI0	Fdclki0	DCLKI frequency	–	–	80	MHz
	Thdclki0	DCLKI H width	5	–	–	ns
	Tldclki0	DCLKI L width	5	–	–	ns
DCLKI1	Fdclki1	DCLKI frequency	–	–	80	MHz
	Thdclki1	DCLKI H width	5	–	–	ns
	Tldclki1	DCLKI L width	5	–	–	ns
DCLK (internal)	Tldclk0	DCLK frequency (*1)	–	–	80	MHz
DCLK (internal)	Tldclk1	DCLK frequency (*1)	–	–	80	MHz
DCLKO0	Fdclko	DCLKO frequency	–	–	80	MHz
DCLKO1	Fdclko	DCLKO frequency	–	–	80	MHz

*1: Internal display clock of PLL synchronization mode is generated by division of internal PLL in the display clock prescaler.
*2: DCLKI or internal display clock of PLL is output.

8.5.5.2. Input Signal

1) Applied the signal only in PLL synchronization mode (CKS = 0) (Reference clock = Clock output from internal PLL)

Table 8-29 AC Timing of Video Interface Input Signal (1)

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
HSYNC0 (i)	Twhsync0	HSYNC input pulse width	3.0	–	–	Clock
HSYNC1 (i)	Twvsync1	VSYNC input pulse width	3.0	–	–	Clock
VSYNC0 (i)	Twvsync	VSYNC input pulse width	1	–	–	HSYNC
VSYNC1 (i)	Twvsync	VSYNC input pulse width	1	–	–	HSYNC

2) Applied the signal only in DCLKI synchronization mode (CKS = 1) (Reference clock = DCLKI)

Table 8-30 AC Timing of Video Interface Input Signal (2)

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
HSYNC0 (i)	Twhsync0	HSYNC input pulse width	3.0	–	–	Clock
	Tshsync0	HSYNC Input setup time	6.0	–	–	ns
	Thhsync0	HSYNC Input hold time	1.0	–	–	ns
HSYNC1 (i)	Twhsync1	HSYNC input pulse width	3.0	–	–	Clock
	Tshsync1	HSYNC Input setup time	6.0	–	–	ns
	Thhsync1	HSYNC Input hold time	1.0	–	–	ns
VSYNC0 (i)	Twvsync0	VSYNC input pulse width	1	–	–	HSYNC
VSYNC1 (i)	Twvsync1	VSYNC input pulse width	1	–	–	HSYNC

8.5.5.3. Output Signal

Table 8-31 AC Timing of Video Interface Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
DOUTR0[5:0], DOUTG0[5:0], DOUTB0[5:0]	Tdrgb0	RGB output delay time	0	–	5.5	ns
DOUTR1[5:0], DOUTG1[5:0], DOUTB1[5:0]	Tdrgb1	RGB output delay time	0	–	5.5	ns
HSYNC0 (o)	Tdhsync0	HSYNC output delay time	0	–	5.5	ns
HSYNC1 (o)	Tdhsync1	HSYNC output delay time	0	–	5.5	ns
VSYNC0 (o)	Tdvsync0	VSYNC output delay time	0	–	5.5	ns
VSYNC1 (o)	Tdvsync1	VSYNC output delay time	0	–	5.5	ns
CSYNC0	Tdcsync0	CSYNC output delay time	0	–	5.5	ns
CSYNC1	Tdcsync1	CSYNC output delay time	0	–	5.5	ns
GV0	Tdgv0	GV output delay time	0	–	5.5	ns
GV1	Tdgv1	GV output delay time	0	–	5.5	Ns

Note: If hold time is deficient, inverting DCLKO clock is recommended.

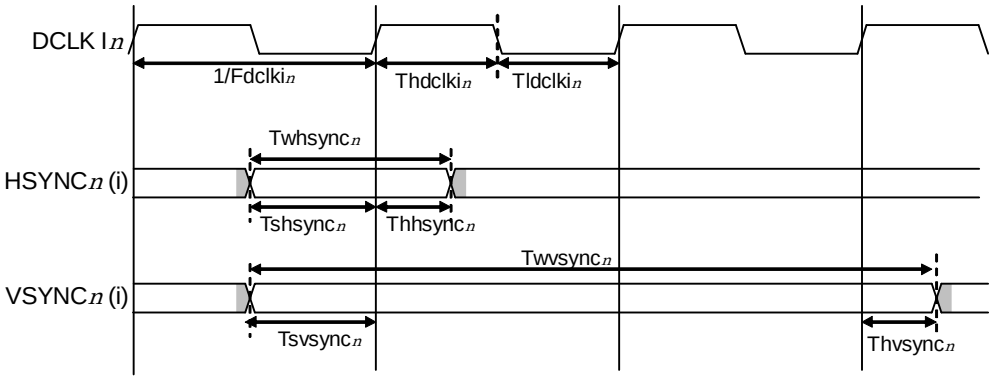


Figure 8-20 Display Input Signal Timing

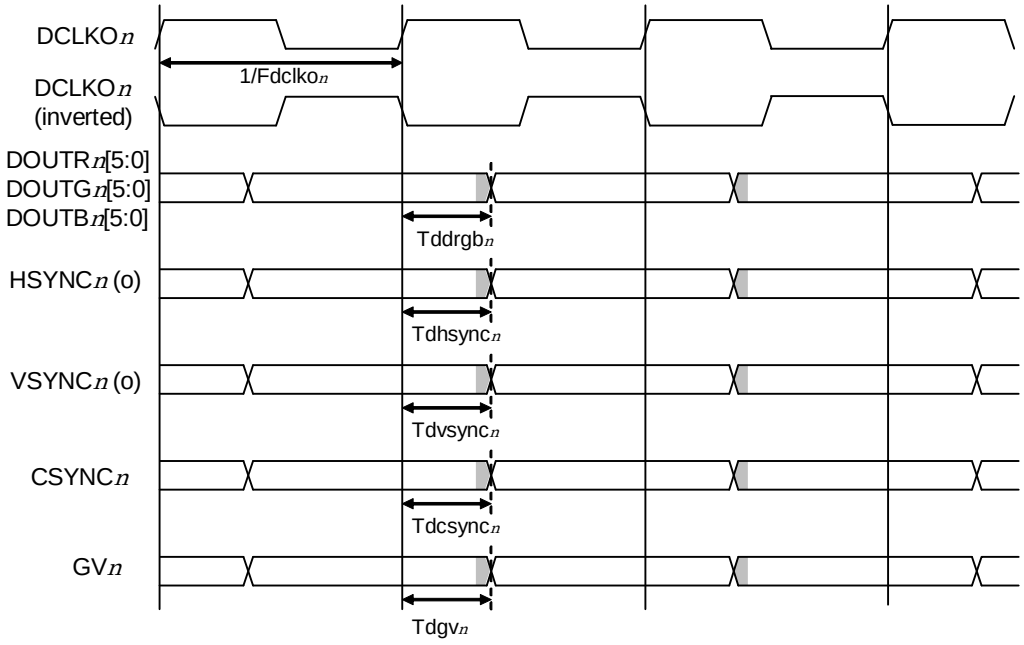


Figure 8-21 Display Output Signal Timing

There is no definition of AC characteristics about analog signal.

8.5.6. GDC Video Capture Signal Timing

8.5.6.1. Clock

Table 8-32 AC Timing of Video Capture Interface Clock Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
CCLK0, CCLK1	f_{CCLK}	Capture clock frequency	–	–	80	MHz
	t_{HCCLK}	Capture clock H width	3	–	–	ns
	t_{LCCLK}	Capture clock L width	3	–	–	ns

Note: It depends on the resolution of the video source.

8.5.6.2. Input Signal

Table 8-33 AC Timing of Video Capture Interface Input Signal

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
VIN0[7:0], VIN1[7:0]	t_{SVI}	Input setup time	6	–	–	ns
	t_{HVI}	Input hold Time	1	–	–	ns
RI1[7:2]	t_{SRI}	Input setup time	6	–	–	ns
	t_{HRI}	Input hold Time	1	–	–	ns
GI1[7:2]	t_{SGI}	Input setup time	6	–	–	ns
	t_{HGI}	Input hold Time	1	–	–	ns
BI1[7:2]	t_{SBI}	Input setup time	6	–	–	ns
	t_{HBI}	Input hold Time	1	–	–	ns
VINHSYNC0, VINHSYNC1	t_{SHSI}	Input setup time	6	–	–	ns
	t_{HHSI}	Input hold Time	1	–	–	ns
VINVSYNC0, VINVSYNC1	t_{SVSI}	Input setup time	6	–	–	ns
	t_{HVSI}	Input hold Time	1	–	–	ns
VINFID0, VINFID1	t_{SFI}	Input setup time	6	–	–	ns
	t_{HFI}	Input hold Time	1	–	–	ns

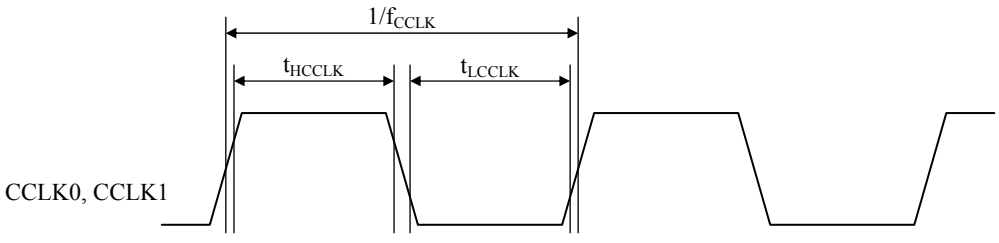


Figure 8-22 Video Capture Clock Input Signal Timing

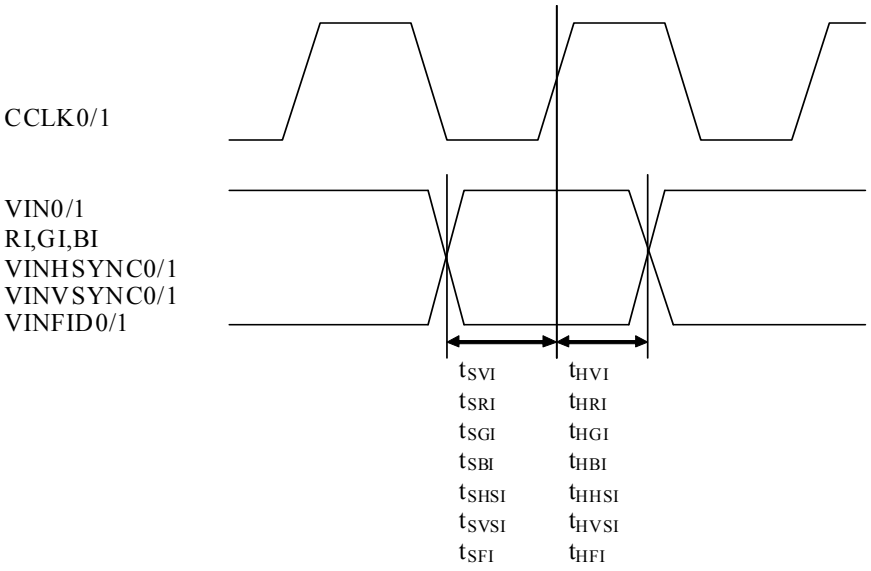


Figure 8-23 Video Capture Input Signal Timing

8.5.7. I2S Signal Timing

Table 8-34 Timing Requirements

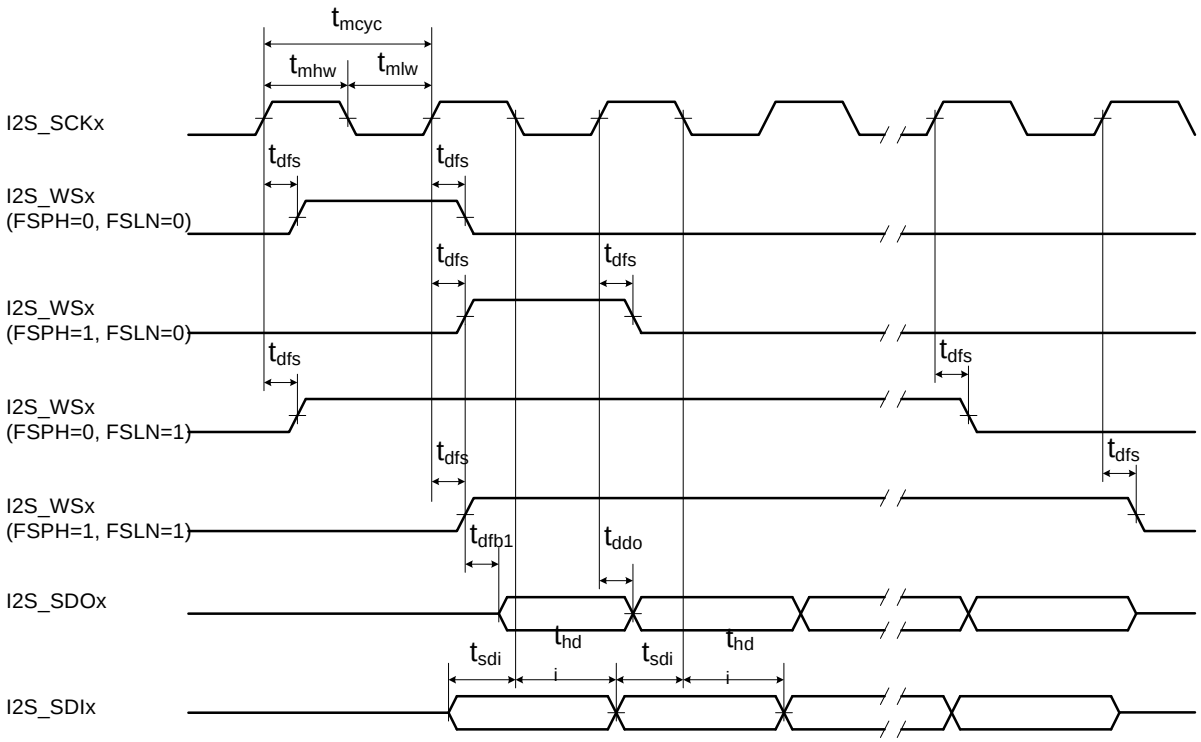
Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2S_SCKx	t_{scyc}	Operating frequency, I2S_SCKx (slave Mode)	–	–	0.5*B	MHz
	t_{shw}	Pulse duration, I2S_SCKx High (slave Mode)	0.45*T	–	0.55*T	ns
	t_{slw}	Pulse duration, I2S_SCKx Low (slave Mode)	0.45*T	–	0.55*T	ns
I2S_WSx	t_{sfi}	Setup time, external I2S_WSx High before I2S_SCKx Low (slave mode)	8	–	–	ns
	t_{hfi}	Hold time, external I2S_WSx High after I2S_SCKx Low (slave Mode)	4	–	–	ns
I2S_SDIx	t_{sdi}	Setup time, I2S_SDIx valid before I2S_SCKx Low (master mode)	8	–	–	ns
		Setup time, I2S_SDIx valid before I2S_SCKx Low (slave Mode)	8	–	–	ns
	t_{hdi}	Hold time, I2S_SDIx valid after I2S_SCKx Low (master mode)	4	–	–	ns
		Hold time, I2S_SDIx valid after I2S_SCKx Low (slave mode)	4	–	–	ns

B indicates AHB bus clock frequency.
T indicates I2S_SCKx cycle.

Table 8-35 Switching Characteristics

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
I2S_SCKx	t_{mcyc}	Operating frequency, I2S_SCKx (master mode)	–	–	0.5*B	MHz
	t_{mhw}	Pulse duration, I2S_SCKx high (master mode)	0.45*T	–	0.55*T	ns
	t_{mlw}	Pulse duration, I2S_SCKx low (master mode)	0.45*T	–	0.55*T	ns
I2S_WSx	t_{dfs}	Delay time, I2S_SCKx High to I2S_WSx transition (master mode)	-12	–	12	ns
I2S_SDOx	t_{ddo}	Delay time, I2S_SCKx High to I2S_SDOx valid except the first bit of transmit frame. (master mode)	-12	–	17	ns
		Delay time, I2S_SCKx high to I2S_SDOx valid except the first bit of transmit frame. (slave mode)	3	–	32	ns
	t_{dfb1}	Delay time, I2S_SCKx high to the first bit of a transmit frame when FSPH bit of I2Sx_CNTREG register is 1. (master mode)	-14	–	17	ns

B indicates AHB bus clock frequency.
T indicates I2S_SCKx cycle.



FSPH is bit 2 of I2Sx_CNTREG register.

FSLN is bit 1 of I2Sx_CNTREG register.

Figure 8-24 Master Mode Timing

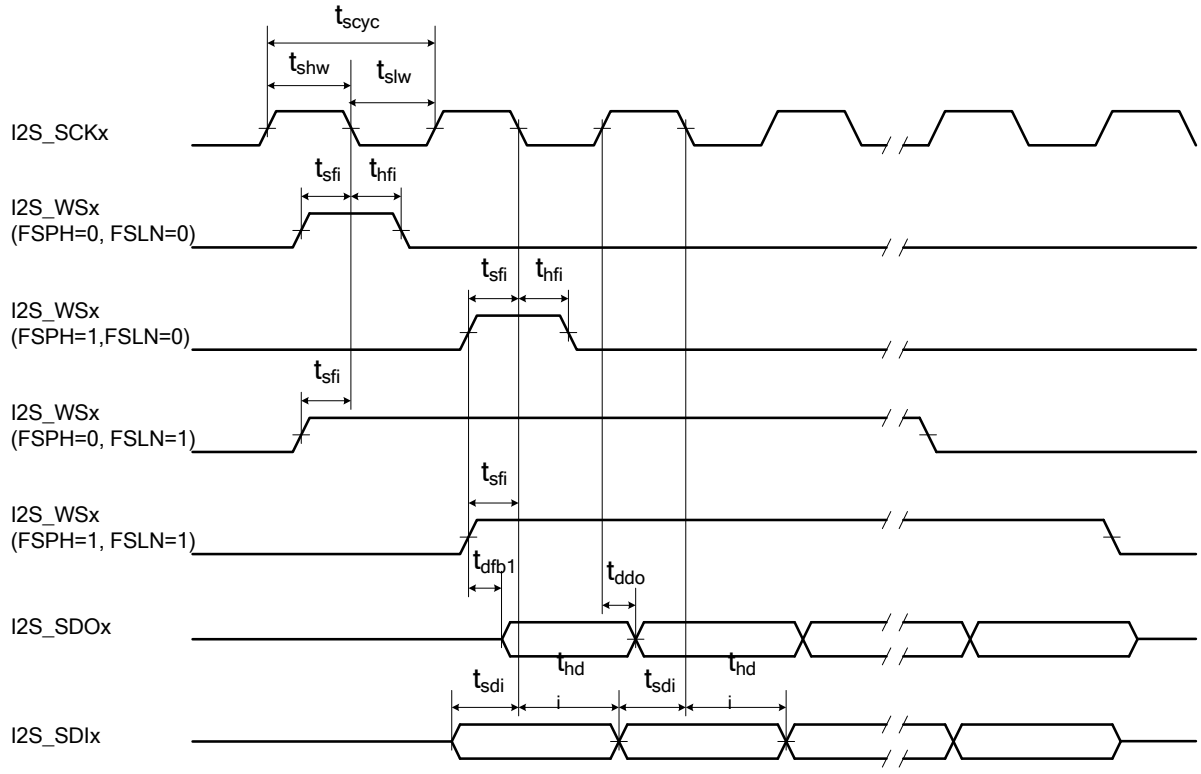


Figure 8-25 Slave Mode Timing

8.5.8. UART Signal Timing

Table 8-36 AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
UART_SOUT0 UART_SOUT1 UART_SOUT2 UART_SOUT3 UART_SOUT4 UART_SOUT5	t_{do}	Data output delay time	–	–	12	ns
UART_SIN0 UART_SIN1 UART_SIN2 UART_SIN3 UART_SIN4 UART_SIN5	t_{dw}	Input data width	16*A	–	–	ns
UART_XRTS0	t_{rtso}	XRTS output delay time	–	–	11	ns
UART_XCTS0	t_{ctsw}	Input XCTS data width	A	–	–	ns

Internal clock is the standard of output delay.
A indicates APB bus clock cycle, and it is different from the output delay standard clock.

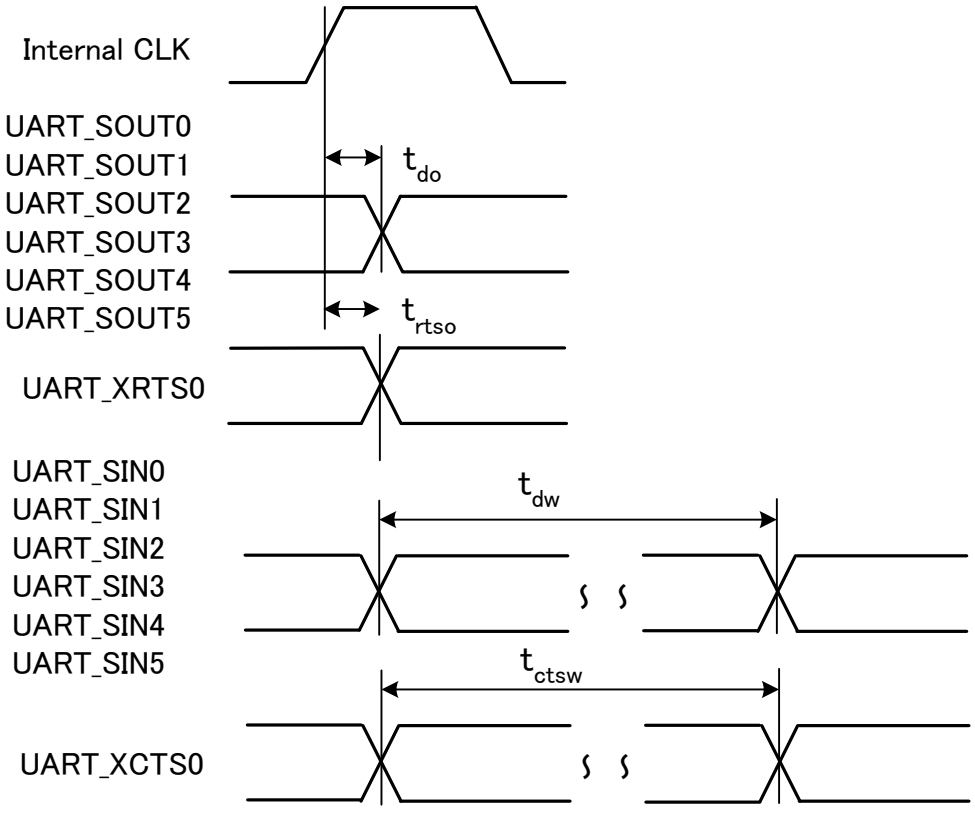


Figure 8-26 UART Timing

8.5.9. I²C Bus Timing

Table 8-37 AC timing of I²C signal

Signal	Symbol	Description		Value			Unit
				Min.	Typ.	Max.	
I2C_SDA0 I2C_SDA1	T_{S2SDAI}	SDAI setup time	Normal mode	250 (*1)	–	–	ns
			High-speed mode	100 (*1)	–	–	ns
	T_{H2SDAI}	SDAI hold time	Normal mode	0.0 (*1)	–	–	ns
			High-speed mode	0.0 (*1)	–	–	ns
	T_{WBFI}	BUS free time	Normal mode	4.7 (*1)	–	–	µs
			High-speed mode	1.3 (*1)	–	–	µs
I2C_SCL0 I2C_SCL1	T_{CSCLI}	SCLI cycle time	Normal mode	1.0 (*1)	–	–	µs
			High-speed mode	2.5 (*1)	–	–	µs
	T_{WHSCLI}	SCLI H width	Normal mode	4.0 (*1)	–	–	µs
			High-speed mode	0.6 (*1)	–	–	µs
	T_{WLSCLI}	SCLI L width	Normal mode	4.7 (*1)	–	–	µs
			High-speed mode	1.3 (*1)	–	–	µs
	T_{CSCLO}	SCLO cycle time	Normal mode	2*m + 2 (*2)	–	–	PCLK (*3)
			High-speed mode	Int (1.5*m) + 2 (*2)	–	–	PCLK (*3)
	T_{WHSCLO}	SCLO H width	Normal mode	m + 2 (*2)	–	–	PCLK (*3)
			High-speed mode	Int (0.5*m) + 2 (*2)	–	–	PCLK (*3)
	T_{WLSCLO}	SCLO L width	Normal mode	m (*2)	–	–	PCLK (*3)
			High-speed mode	m (*2)	–	–	PCLK (*3)
	T_{S2SCLI}	SCLI setup time	Normal mode	4.0 (*2)	–	–	µs
			High-speed mode	0.6 (*2)	–	–	µs
	T_{H2SCLI}	SCLI hold time	Normal mode	4.7 (*2)	–	–	µs
			High-speed mode	1.3 (*2)	–	–	µs

*1: I²C bus specification value
*2: See I²C bus interface's clock control register (I2CxCCR) of the MB86R01 LSI product specifications for the "m" value
*3: PCLK = APB bus clock cycle

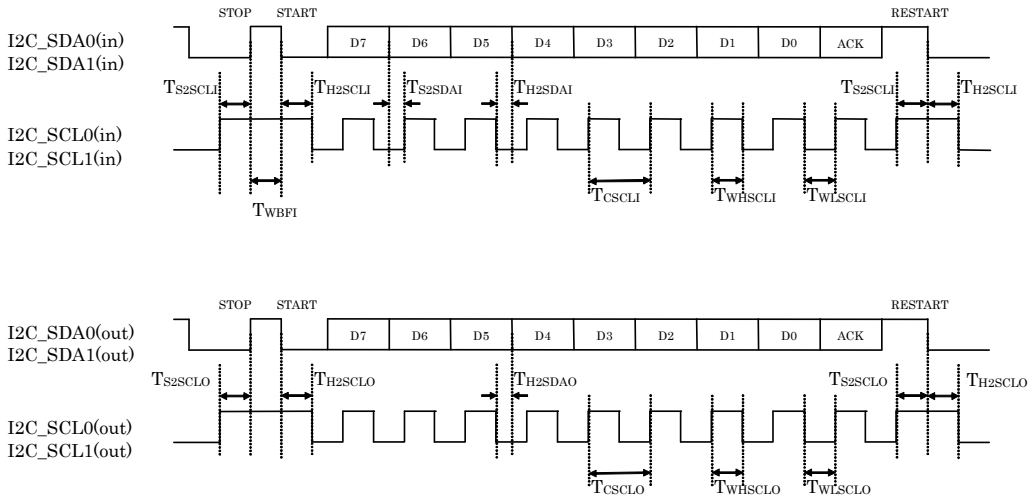


Figure 8-27 I²C Access Timing

8.5.10. SPI Signal Timing

Table 8-38 SPI AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SPI_SCK	t_{cyc}	Operating frequency	–	–	0.5*A	MHz
SPI_DI	t_{sdi}	Setup time, SPI_DI valid before SPI_SCK	15	–	–	ns
	t_{hdi}	Hold time, SPI_DI valid after SPI_SCK	15	–	–	ns
SPI_DO	t_{do}	Delay time, SPI_SCK	-2	–	5	ns
SPI_SS	t_{sso}	Delay time, SPI_SCK	-2	–	5	ns

A indicates APB bus clock frequency.

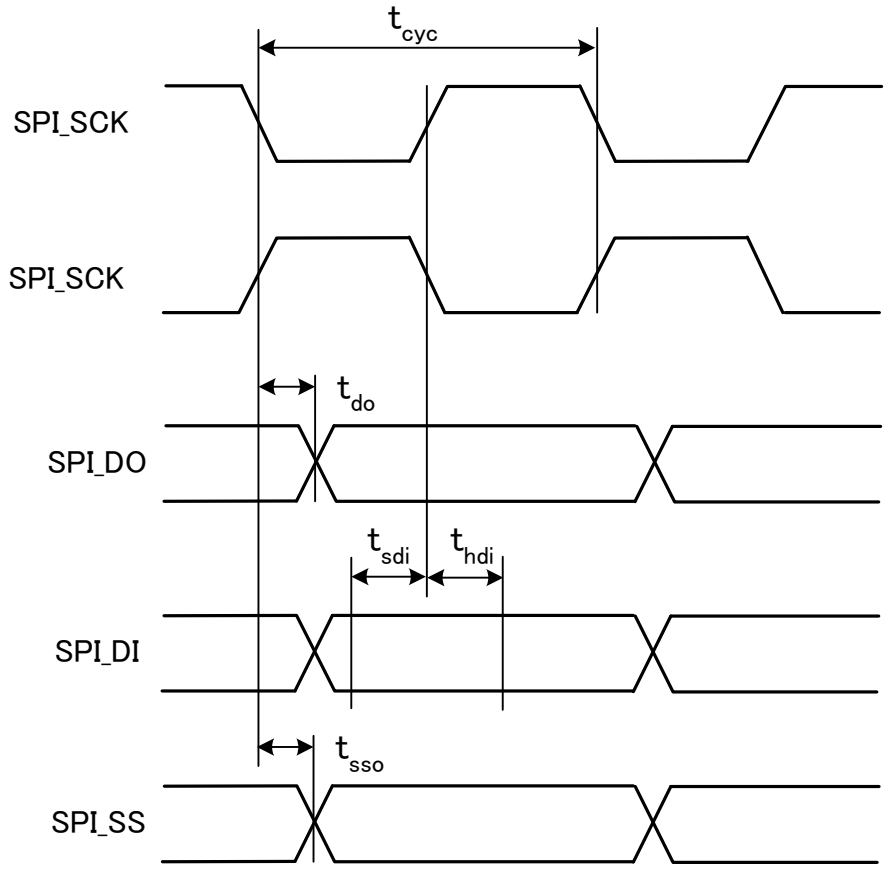


Figure 8-28 SPI Timing

Polarity of SPI_SCK is determined by the register setting.

8.5.11. CAN Signal Timing

Table 8-39 CAN AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
CAN_TX0 CAN_TX1	t_{do}	Data output delay time	–	–	17	ns
CAN_RX0 CAN_RX1	t_{dw}	Input data width	1000	–	–	ns

Internal clock is the standard of output delay.

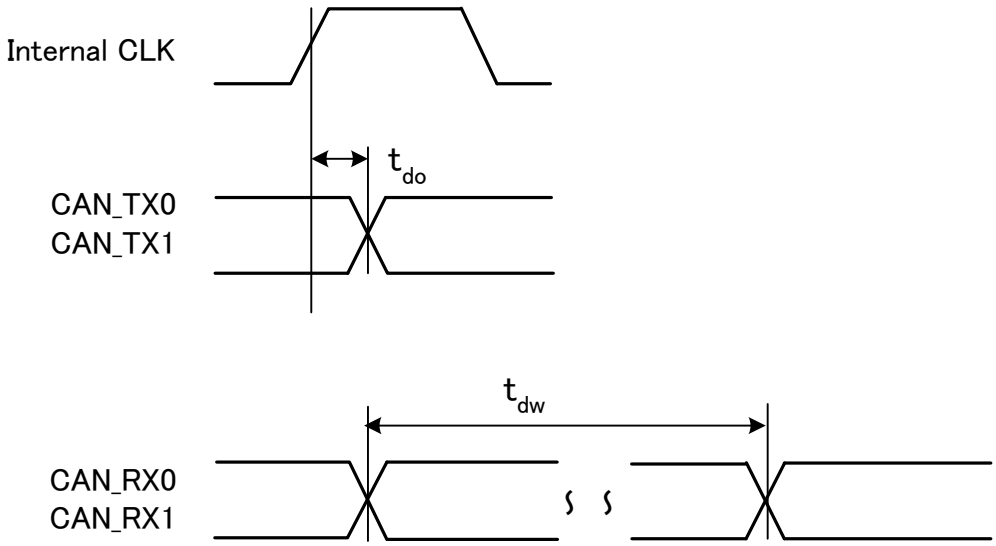


Figure 8-29 CAN Timing

8.5.12. MediaLB Signal Timing

8.5.12.1. MediaLB AC Spec Type A

Ground = 0V; Load capacitance = 60pF; MediaLB speed = 256Fs or 512Fs; Fs = 48kHz; all timing parameters specified from the valid voltage threshold as listed below; unless otherwise noted.

8.5.12.1.1. Clock

Table 8-40 AC Timing of Clock Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBCLK	f_{mck}	MLBCLK operating frequency (*1)	11.264 – –	– 22.5792 –	– – 24.6272	MHz	256xFs at 44.0kHz 512xFs at 44.1kHz 512xFs at 48.1kHz
	t_{mckr}	MLBCLK rising time	–	–	3	ns	V_{IL} to V_{IH}
	t_{mckf}	MLBCLK falling time	–	–	3	ns	V_{IH} to V_{IL}
	t_{mckc}	MLBCLK cycle time	– –	81 40	– –	ns	256xFs 512xFs
	t_{mckl}	MLBCLK low time	30 14	37 17	– –	ns	256xFs 512xFs
	t_{mckh}	MLBCLK high time	30 14	38 17	– –	ns	256xFs 512xFs
	t_{mpwv}	MLBCLK pulse width variation	–	–	2	ns pp	(*2)

*1: The controller can shut off MLBCLK to place MediaLB in a low-power state.
*2: Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

8.5.12.1.2. Input Signal

Table 8-41 AC Timing of Input Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT input	t_{dsmcf}	MLBSIG and MLBDAT input valid to MLBCLK falling	4	–	–	ns	
	t_{dhmcf}	MLBSIG and MLBDAT input hold from MLBCLK low	0	–	–	ns	

8.5.12.1.3. Output Signal

Table 8-42 AC Timing of Output Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT output	t_{mcfdz}	MLBSIG and MLBDAT output high impedance from MLBCLK low	0	–	t_{mckl}	ns	
	t_{mdzh}	Bus hold time	4	–	–	ns	(*1)

*1: The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

8.5.12.2. MediaLB AC Spec Type B

Ground = 0V, Load capacitance = 40pF, MediaLB speed = 1024Fs, and Fs = 48kHz.
All timing parameters are specified from the valid voltage threshold as listed below; unless otherwise noted.

8.5.12.2.1. Clock

Table 8-43 AC Timing of Clock Signal

Signal	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBCLK	f_{mck}	MLBCLK operating frequency (*1)	45.056 – –	– 49.152 –	– – 49.2544	MHz	1024xFs at 44.0kHz 1024xFs at 48.0kHz 1024xFs at 48.1kHz
	t_{mckr}	MLBCLK rising time	–	–	1	ns	V_{IL} to V_{IH}
	t_{mckf}	MLBCLK falling time	–	–	1	ns	V_{IH} to V_{IL}
	t_{mckc}	MLBCLK cycle time	–	20.3	–	ns	
	t_{mckl}	MLBCLK low time	6.8	7.8	–	ns	
	t_{mckh}	MLBCLK high time	9.7	10.4	–	ns	
	t_{mpwv}	MLBCLK pulse width variation	–	–	0.5	ns pp	(*2)

*1: The controller can shut off MLBCLK to place MediaLB in a low-power state.
*2: Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp).

8.5.12.2.2. Input Signal

Table 8-44 AC Timing of Input Signal

Signal Name	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT input	t_{dsmcf}	MLBSIG and MLBDAT input valid to MLBCLK falling	1	–	–	ns	
	t_{dhmcf}	MLBSIG and MLBDAT input hold from MLBCLK low	0	–	–	ns	

8.5.12.2.3. Output signal

Table 8-45 AC Timing of Output Signal

Signal Name	Symbol	Description	Value			Unit	Comment
			Min.	Typ.	Max.		
MLBSIG, MLBDAT Output	t_{mcfdz}	MLBSIG and MLBDAT output high impedance from MLBCLK low	0	–	t_{mckl}	ns	
	t_{mdzh}	Bus hold time	2	–	–	ns	(*1)

*1: The board must be designed to ensure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

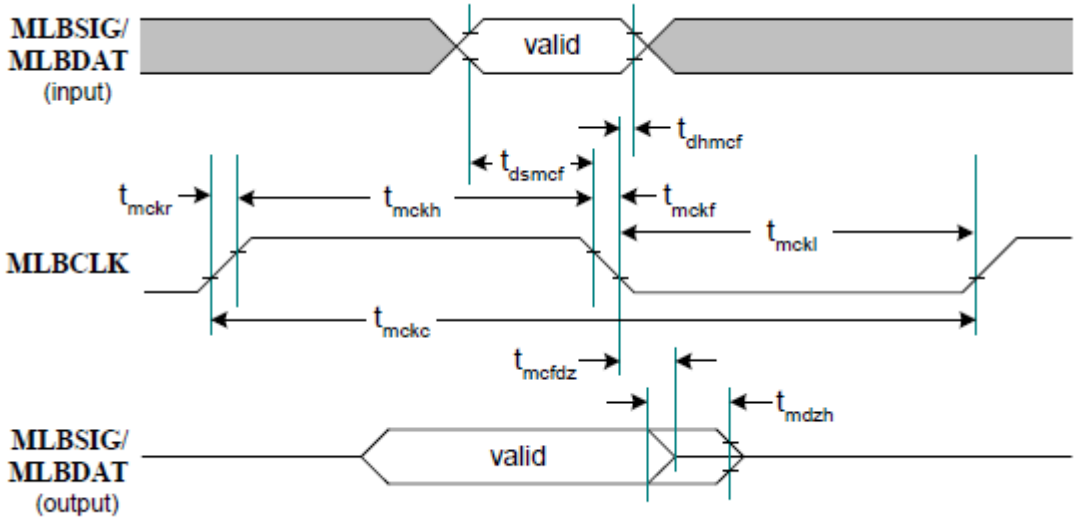


Figure 8-30 MediaLB Timing

Figure 8-31 MediaLB Pulse Width Variation Timing

8.5.13. USB2.0 Signal Timing

Table 8-46 High-speed AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
USB_HSDP USB_HSDM USB_FSDP USB_FSDM	Driver characteristics:					
	t_{hsr}	Rise time (10% - 90%)	500	–	–	ps
	t_{hsf}	Fall time (10% - 90%)	500	–	–	ps
	–	Driver waveform requirements	Complying with USB2.0 specification (section 7.1.2)			
	zhsdrv	Driver output resistance (which also serves as high-speed termination)	40.5	–	49.5	Ω
	Clock timing:					
	thsdrat	High-speed data rate	479.760	–	480.240	Mb/s
	High-speed data timing:					
	–	Data source jitter	Complying with USB2.0 specification (section 7.1.2)			
	–	Receiver jitter tolerance				

Table 8-47 Full-speed AC Timing

Signal	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
USB_HSDP USB_HSDM USB_FSDP USB_FSDM	Driver characteristics:					
	t_{fr}	Rise time (10% - 90%)	4	–	20	ns
	t_{ff}	Fall time (10% - 90%)	4	–	20	ns
	t_{frfm}	Difference rise and fall time matching	90	–	111.11	%
	Clock timing: (in case of using UTMI i/f and setting FSSEL = "0")					
	$t_{fdraths}$	Full-speed data rate for hubs and devices which are capable of high-speed	11.9940	–	12.0060	Mb/s
	Full-speed data timings: (in case of using UTMI i/f and setting FSSEL = "0")					
	t_{dj1} t_{dj2}	Source jitter total (including frequency tolerance): To next transition For paired transitions	 -3.5 -4	 – –	 3.5 4	ns
	t_{fdeop}	Source jitter for differential transition to SE0 transition	-2	–	5	ns
	t_{jr1} t_{jr2}	Receiver jitter: To next transition For paired transitions	 -18.5 -9	 –	 18.5 9	ns
	t_{feopt}	Source SE0 interval of EOP	160	–	175	ns
	t_{feopr}	Receiver SE0 interval of EOP	82	–	–	ns
	t_{fst}	Width of SE0 interval during differential transition	–	–	14	ns

Table 8-48 Low-speed AC Timing

Signal	**Symbol**	**Description**	**Value**			**Unit**
			Min.	**Typ.**	**Max.**	
USB_HSDP USB_HSDM USB_FSDP USB_FSDM	Driver characteristics:					
	t_{lr}	Rise time (10% - 90%)	75	–	300	ns
	t_{lf}	Fall time (10% - 90%)	75	–	300	ns
	t_{lrfm}	Rise and fall time matching	80	–	125	%

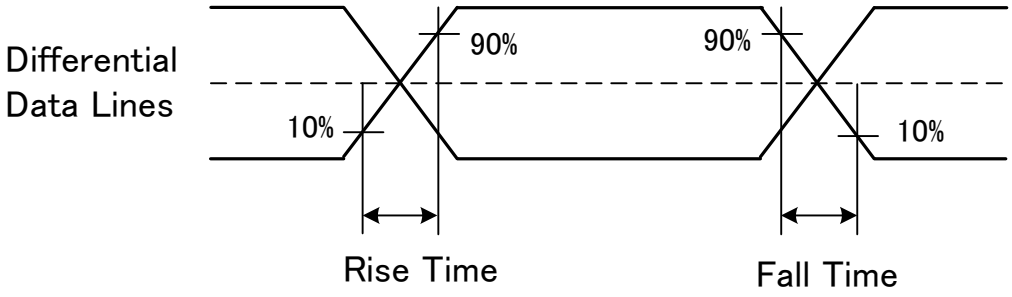


Figure 8-32 Data Signal Rise and Fall Time

8.5.14. IDE66 Signal Timing

8.5.14.1. IDE PIO Timing

Table 8-49 AC timing of Register Access

Symbol	Description	Value					Unit
		mode0	mode1	mode2	mode3	mode4	
t0	Cycle time (min.)	600	383	330	180	120	ns
t1	Address valid to IDE_XDIOR/IDE_XDIOW setup (min.)	70	50	30	30	25	ns
t2	IDE_XDIOR/IDE_XDIOW pulse width 8 bit (min.)	290	290	290	80	70	ns
t2i	IDE_XDIOR/IDE_XDIOW recovery time (min.)	–	–	–	70	25	ns
t3	IDE_XDIOW data setup (min.)	60	45	30	30	20	ns
t4	IDE_XDIOW data hold (min.)	30	20	15	10	10	ns
t5	IDE_XDIOR data setup (min.)	50	35	20	20	20	ns
t6	IDE_XDIOR data hold (min.)	5	5	5	5	5	ns
t6Z	IDE_XDIOR data tristate (max.)	30	30	30	30	30	ns
t9	IDE_XDIOR/IDE_XDIOW to address valid hold (min.)	20	15	10	10	10	ns
tRD	Read data valid to IDE_DIORDY active (if IDE_DIORDY initially low after tA) (min.)	0	0	0	0	0	ns
tA	IDE_DIORDY setup time	35	35	35	35	35	ns
tB	IDE_DIORDY pulse width (max.)	1250	1250	1250	1250	1250	ns
tC	IDE_DIORDY assertion to release (max.)	5	5	5	5	5	ns

Table 8-50 AC timing of Data Access

Symbol	Description	Value					Unit
		mode0	mode1	mode2	mode3	mode4	
t0	Cycle time (min.)	600	383	240	180	120	ns
t1	Address valid to IDE_XDIOR/IDE_XDIOW setup (min.)	70	50	30	30	25	ns
t2	IDE_XDIOR/IDE_XDIOW pulse width 8 bit (min.)	165	125	100	80	70	ns
t2i	IDE_XDIOR/IDE_XDIOW recovery time (min.)	–	–	–	70	25	ns
t3	IDE_XDIOW data setup (min.)	60	45	30	30	20	ns
t4	IDE_XDIOW data hold (min.)	30	20	15	10	10	ns
t5	IDE_XDIOR data setup (min.)	50	35	20	20	20	ns
t6	IDE_XDIOR data hold (min.)	5	5	5	5	5	ns
t6Z	IDE_XDIOR data tristate (max.)	30	30	30	30	30	ns
t9	IDE_XDIOR/IDE_XDIOW to address valid hold (min.)	20	15	10	10	10	ns
tRD	Read data valid to IDE_DIORDY active (if IDE_DIORDY initially low after tA) (min.)	0	0	0	0	0	ns
tA	IDE_DIORDY setup time	35	35	35	35	35	ns
tB	IDE_DIORDY pulse width (max.)	1250	1250	1250	1250	1250	ns
tC	IDE_DIORDY assertion to release (max.)	5	5	5	5	5	ns

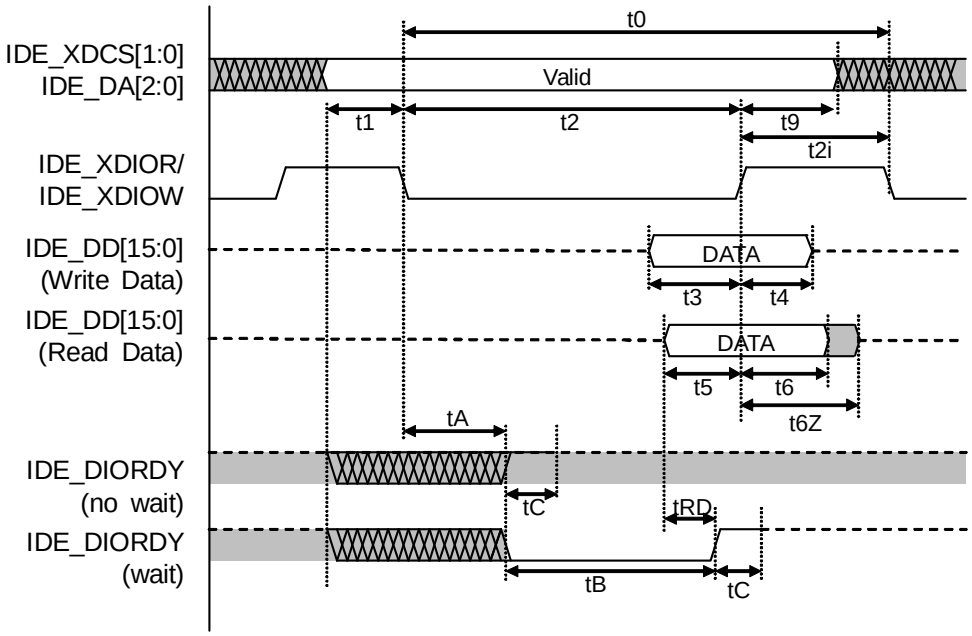


Figure 8-33 PIO Access Timing

8.5.14.2. IDE Ultra DMA Timing

Table 8-51 AC timing of Ultra DMA

Symbol	Description	Value										Unit
		mode0		mode1		mode2		mode3		mode4		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
T2cycleTYP	Typical sustained average 2 cycle time	240	–	160	–	120	–	90	–	60	–	ns
T2cycle	2 cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	–	154	–	115	–	86	–	57	–	ns
Tcycle	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	–	73	–	54	–	39	–	25	–	ns
Tdvs	Data valid setup time at sender (from data valid until STROBE edge)	70	–	48	–	30	–	20	–	6.7	–	ns
Tdvh	Data valid setup time at sender (from STROBE edge until data may become invalid)	6.2	–	6.2	–	6.2	–	6.2	–	6.2	–	ns
Tfs	First STROBE time (for device to first negateDSTROBE from STOP during data in Burst)	–	230	–	200	–	170	–	130	–	120	ns
Tli	Limited interlock time	0	150	0	150	0	150	0	100	0	100	ns
Tmli	Interlock time with minimum	20	–	20	–	20	–	20	–	20	–	ns
Tui	Unlimited interlock time	0	–	0	–	0	–	0	–	0	–	ns
Taz	Maximum time allowed for output drivers to release (from asserted or negated)	–	10	–	10	–	10	–	10	–	10	ns
Tzah	Minimum delay time required for output	20	–	20	–	20	–	20	–	20	–	ns
Tzad	Drivers to assert or negate (from released)	0	–	0	–	0	–	0	–	0	–	ns
Tenv	Envelope time (from DMACK- to STOP and HDMARDY- during data in burst initiation and from IDE_XDDDMACK to STOP during data out burst initiation)	20	70	20	70	20	70	20	55	20	55	ns
Trfs	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY)	–	75	–	70	–	60	–	60	–	60	ns
Trp	Minimum time to assert STOP or negate IDE_DMARQ	160	–	125	–	100	–	100	–	100	–	ns
Tiordyz	Maximum time before releasing IDE_DIORDY	–	20	–	20	–	20	–	20	–	20	ns
tziordy	Minimum time before driving STROBE	0	–	0	–	0	–	0	–	0	–	ns
Tack	Setup and hold times for DMACK- (before assertion or negation)	20	–	20	–	20	–	20	–	20	–	ns
Tss	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates burst)	50	–	50	–	50	–	50	–	50	–	ns

<Ultra DMA Read Access>

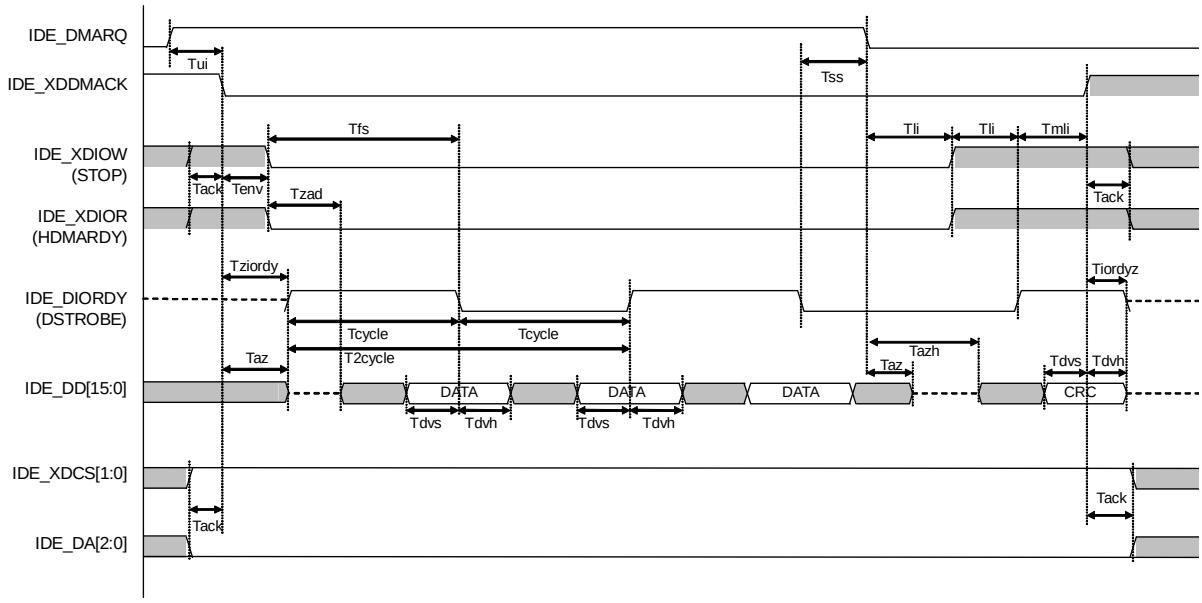


Figure 8-34 IDE Read Access Timing

<Ultra DMA Write Access>

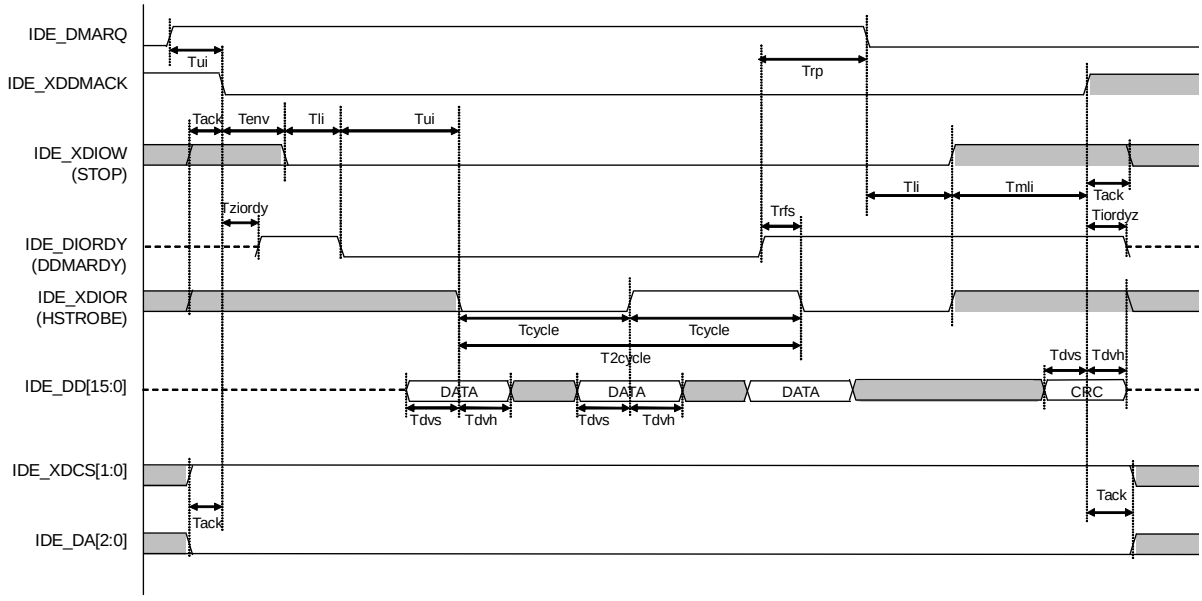


Figure 8-35 IDE Write Access Timing

8.5.15. SD Signal Timing

8.5.15.1. Clock

Table 8-52 AC Timing of Clock Signal

Signal Name	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SD_CLK	t_CLK	SD_CLK cycle	–	–	20.83 (*1)	MHz

*1: 20.83MHz for SD memory card and 20MHz for multimedia card (MMC)

8.5.15.2. Input/Output Signal

Table 8-53 AC Timing of Data Signal

Signal Name	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
SD_DAT[3:0]	tD_DAT	Output data delay (standard of SD_CLK falling edge)	-6.0	–	3.0	ns
	tS_DAT	Input data setup (standard of SD_CLK rising edge)	13.0	–	–	ns
	tH_DAT	Input data hold (standard of SD_CLK rising edge)	19.0	–	–	ns

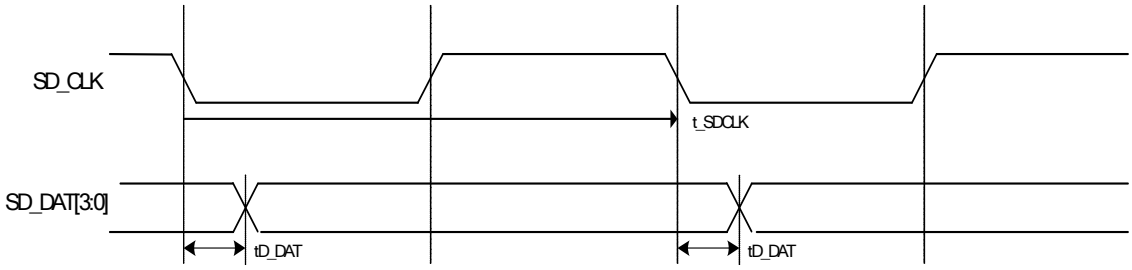


Figure 8-36 Output Timing to Media

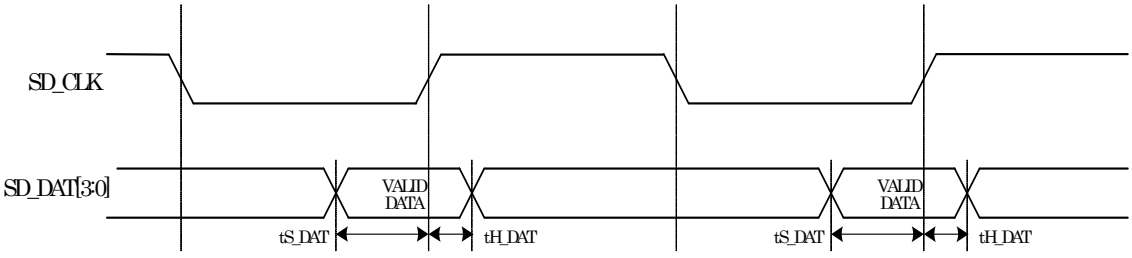
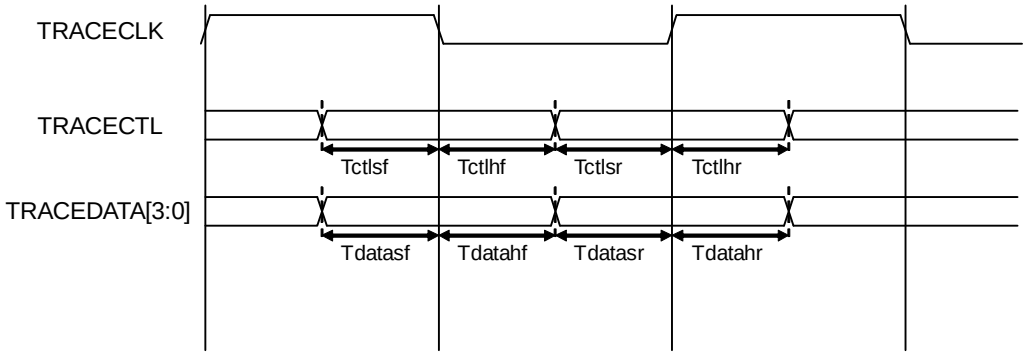


Figure 8-37 Input Timing from Media

8.5.16. ETM9 Trace Port Signal Timing

Table 8-54 AC Timing of Trace Signal

Signal Name	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
TRACECTL	Tctlsr	TRACECTL setup time to rising edge of TRACECLK.	2	–	–	ns
	Tctlhr	TRACECTL hold time to rising edge of TRACECLK.	1	–	–	ns
	Tctlsf	TRACECTL setup time to falling edge of TRACECLK.	2	–	–	ns
	Tctlhf	TRACECTL hold time to falling edge of TRACECLK.	1	–	–	ns
TRACEDATA[3:0]	Tdatasr	TRACEDATA setup time to rising edge of TRACECLK.	2	–	–	ns
	Tdatahr	TRACEDATA hold time to rising edge of TRACECLK.	1	–	–	ns
	Tdatasf	TRACEDATA setup time to falling edge of TRACECLK.	2	–	–	ns
	Tdatahf	TRACEDATA hold time to falling edge of TRACECLK.	1	–	–	ns



[NOTE] MB86R01 supports only half-rate clocking mode.

Figure 8-38 Trace Signal Timing

8.5.17. EXIRC Signal Timing

Table 8-55 AC Timing

Signal Name	Symbol	Description	Value			Unit
			Min.	Typ.	Max.	
INT_A[3:0]	t_{dw}	Input data-width	A	–	–	ns

The case that external interrupt input request is edge (rising edge and falling edge), input data width (tdw) is regulated as follows. When level ("H" or "L") is selected as the request, it should be held until interrupt process is completed.
A indicates APB bus clock cycle.

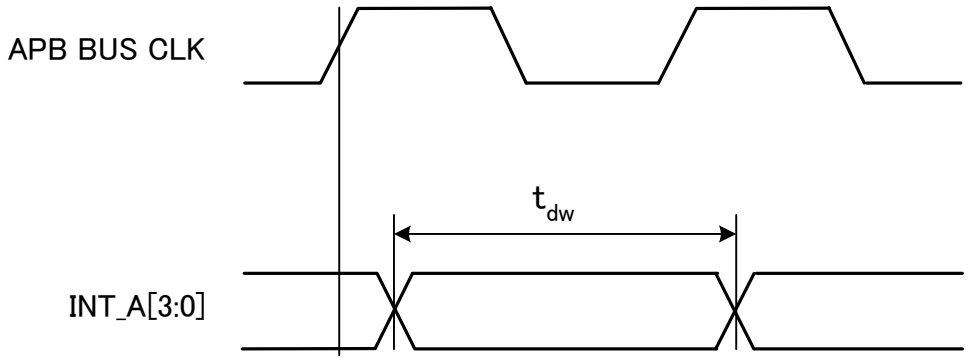
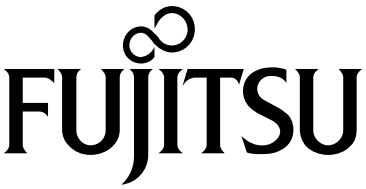


Figure 8-39 EXIRC Timing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